

VME LUPO

Logic Unit for Programmable Operation

Components

- User FPGA = Xilinx Spartan 3E (XC3S500E)
- Configuration PROM (XCF04S)
- VME Interface (CPLD)
- 50 MHz Crystal Oscillator

VME Interface

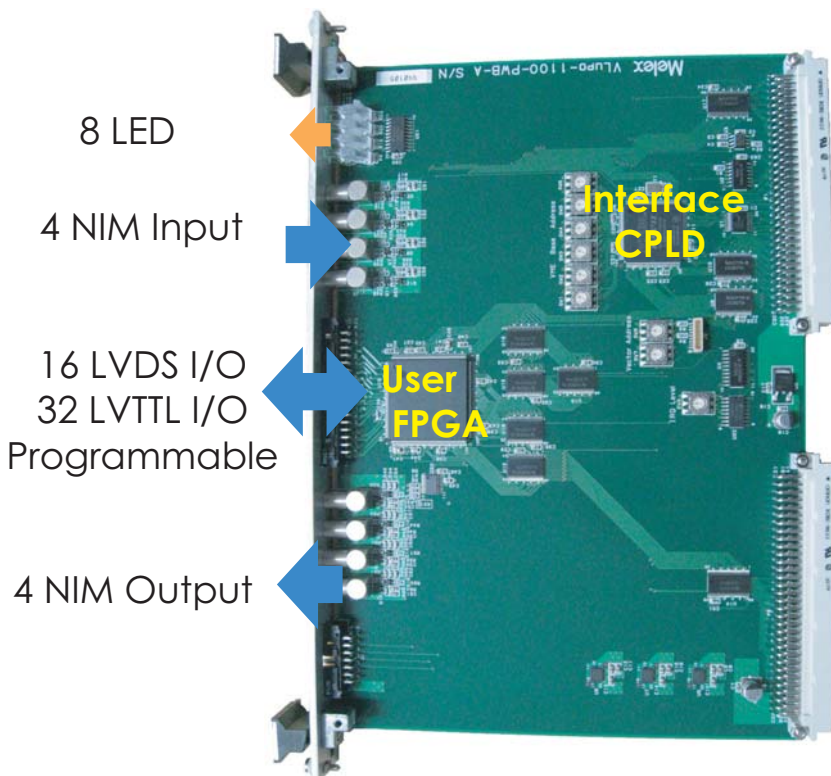
- A32 D32/D16 Mode
- PIO only (BLT is now under development)
- VME Interrupt

FPGA Specification

- 500K System gate
- 45 KB Block RAM
- 4 DCM (Digital Clock Manager)

Application

- Input Register
- Output Register
- Interrupt Register
- NIM-LVDS Level Shifter
- Scaler
- Time Stamper
- Trigger Selector
- Gate and Delay Generator
- FPGA based TDC



Pulse width and delay are programmable (clock sync). Functions are unitable (e.g. I/O and Interrupt register). FIFO memory is available in FPGA. DCM can generate desired clock frequency (e.g. convert 50 MHz clock to 200 MHz clock).