LUPO Multi TimeStamp Module (Ver. 2.0)

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September 26, 2012

1   General

1.1   Function

This module is a CAMAC/VME LUPO module which including the function of Multi-Channel Time stamper, interrupt register, output register.

1.2   Time stamp

Time-stamp values are obtained with a 48 bits depth and a 10 ns resolution according to the trigger inputs (LVDS IN0–15). It can be stored up to 4095 time-stamps into FIFO memory. A 10 ns separation is required to detect subsequent triggers. Input signals have to more than 20 ns width. Both clock sources of internal and external are available. In case of external clock, 100 MHz clock is generated by DLL (Delay Lock Loop) circuit from 25 MHz external clock of NIM IN3. The clear input (NIM IN2) reset the time-stamp value. By using this clear signal, the synchronization for multiple LUPOs are achieved.

1.3   Output register

As a output register, NIM OUT0 can fire pulse and level signals. The width of NIM pulse is variable, and it can be changed 20ns–1.3ms with 20 ns step.

1.4   Interrupt register

As a interrupt register, this module can generate the interrupt signal to VME/CAMAC. The delay time between trigger signal and interrupt generation is variable, and it can be changed 20ns–1.3ms with 20ns step. By the clear command, this interrupt signal is cleared.

1.5   Indicator

1.5.1   Ex Clock OK

When the external clock is correct, this LED lights up. However even if the external clock is not 25 MHz, sometimes this LED becomes ON. And also, after the correct operation, even if cable is removed, sometimes this LED still lights up. When the external clock mode, please check the Ex Clock through output by oscilloscope. If this signal is 25 MHz, the external clock synchronization is correct.

1.5.2   FIFO Full

There is FIFO memory, and it can store 4095 time-stamps. When FIFO becomes full, this LED will light up.

1.5.3   Int/Ext clock mode

With the external clock mode, this LED lights up. Internal clock mode case, this LED is off. The default setting is the external clock mode.

1.6   Connector

1.6.1   NIM input ch0 : Interrupt

CAMAC/VME interrupt signal is generated by this interrupt input. Interrupt is generated by this input signal *OR* when exceed 1024 time-stamps in the FIFO.

1.6.2   NIM input ch1 : Veto

When veto is on, triggers are inhibited.

1.6.3   NIM input ch2 : Time Reset

With this input, time stamp values are cleared to be 0. This input is for the module synchronization. More than 20 ns width logic pulse is required.

1.6.4   NIM input ch3 : Ext Clock

Input external clock. Duty ratio 50:50, 25 MHz NIM logic pulse is needed.

1.6.5   NIM output ch0 : Output 0

An output for NIM level and pulse.

1.6.6   NIM output ch1 : Full

When FIFO buffer is full, NIM level signal is generated.
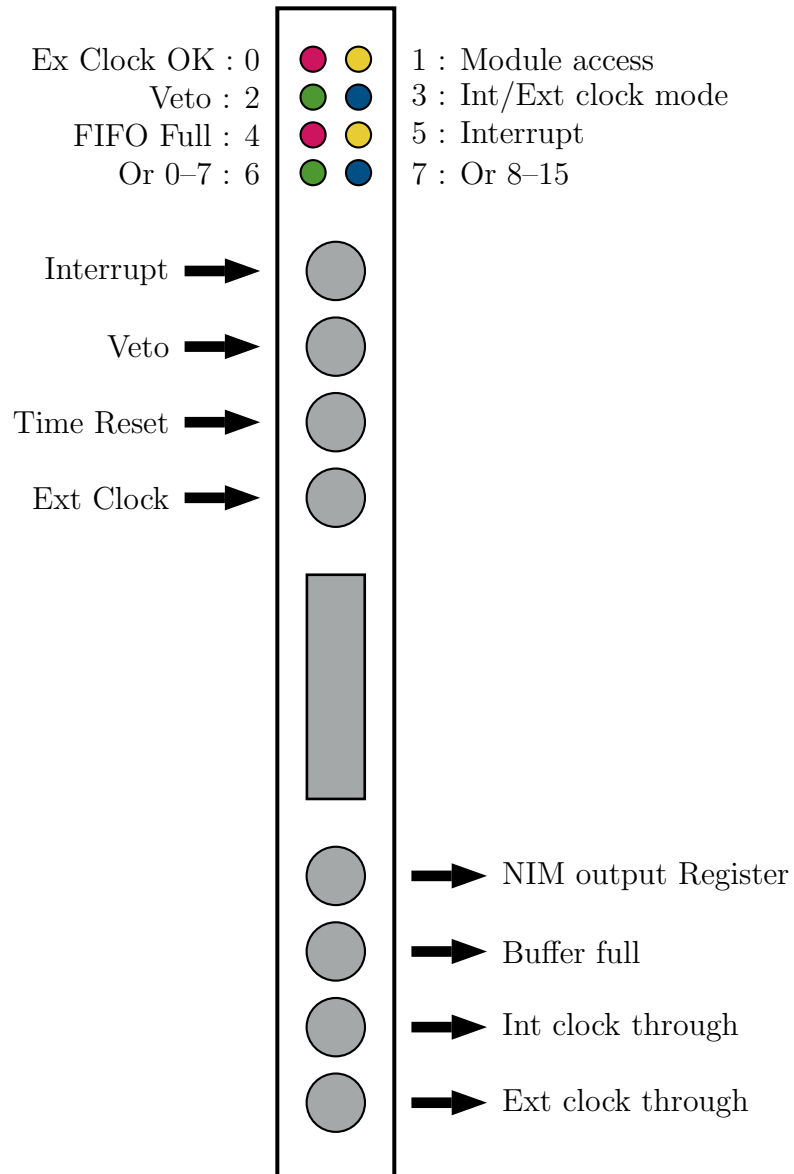
1.6.7   NIM output ch2 : Int clock through

An output of internal 25 MHz clock which is based on internal 50 MHz clock. This signal is used for synchronizing other modules.

1.6.8   NIM output ch3 : Ext clock through

An output signal of external 25 MHz clock which is the through out of the external 25 MHz clock input. This signal is used for checking the external clock quality and synchronizing other modules. This through out is not a real direct output of the external clock. The external clock is put into the DLL circuit once, and this signal come from one of the DLL outputs. Thus, if the 25 MHz external clock has large noise, this through out will be not stable signal.

1.7 Front panel

Ex Clock OK : 0 🔴 🟡 1 : Module access
Veto : 2 🟢 🔵 3 : Int/Ext clock mode
FIFO Full : 4 🔴 🟡 5 : Interrupt
Or 0–7 : 6 🟢 🔵 7 : Or 8–15

Interrupt ➡

Veto ➡

Time Reset ➡

Ext Clock ➡

➡ NIM output Register

➡ Buffer full

➡ Int clock through

➡ Ext clock through

2 Interface

2.1 Register map

Command list.

CAMAC (R/W)		VME	Register	Data	VME R/W
F(0)A(0)		Base + %00	Data Read	D32	read
F(1)A(0)		Base + %10	FIFO Counter	D32	read
F(1)A(2)		Base + %14	FIFO Full Count	D32	read
F(2)A(0)		Base + %20	Data on the fly	D32	read
F(2)A(2)		Base + %24	Clock 10MHz	D32	read
F(2)A(4)		Base + %28	Clock 10KHz	D32	read
F(2)A(6)		Base + %2c	Clock 1KHz	D32	read
	F(16)A(0)	Base + %00	Level Output	D16	write
	F(17)A(0)	Base + %10	Pulse Output	D16	write
F(4)A(0)	F(20)A(0)	Base + %40	Pulse Width	D16	read/write
F(4)A(1)	F(20)A(1)	Base + %42	Interrupt Delay	D16	read/write
F(4)A(2)	F(20)A(2)	Base + %44	Interrupt Source	D16	read/write
F(6)A(0)	F(22)A(0)	Base + %60	Clock Source	D16	read/write
F(6)A(1)	F(22)A(1)	Base + %62	Software Veto	D16	read/write
F(7)A(0)		Base + %70	Module version	D16	read
F(9)A(0)		Base + %90	Clear Interrupt & Interrupt	D16	read
F(9)A(1)		Base + %92	Reset Time Stamp	D16	read
F(9)A(2)		Base + %94	Clear FIFO	D16	read
F(9)A(3)		Base + %96	Clear All	D16	read
F(9)A(4)		Base + %98	Clear Clock	D16	read
	F(24)A(0)	Base + %80	Disable Interrupt	D16	write
	F(26)A(0)	Base + %A0	Enable Interrupt	D16	write

2.1.1 Data Read

F(0)A(0) / Base+%00 D32R Read data from FIFO. 32 bit in VME, 16 bit in CAMAC. In

VME case, first readout returns lower 32 bit value. Second readout returns upper 16 bit value and channel number.

First readout

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Time Stamp															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Time Stamp															

Second readout

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
												Channel			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Time Stamp															

2.1.2   FIFO Counter

F(1)A(0) / Base+%10 D32R

Return the number of 32 bit data in FIFO. The maximum value is 8190.

2.1.3   FIFO Full count

F(1)A(2) / Base+%14 D32R

When FIFO becomes full, this counter is incremented. The counter value is cleared by accessing "Clear FIFO" or "Clear All".

2.1.4   Data on the fly

F(2)A(0) / Base+%20 D32R

Return the current time stamp counter (higher 24 bits).

2.1.5   Level Output

F(16)A(0) / Base+%00 D16W

Output level signals from NIM Output connectors (1=on, 0=off).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															ch0

2.1.6 Pulse Output

F(17)A(0) / Base+%10 D16W

Output pulse signals from NIM Output connectors (1=on, 0=off). With this pulse signal, level output will be canceled.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															ch0

2.1.7 Pulse Width

F(4/20)A(0) / Base+%40 D16RW Set the width of the pulse output signal. 1 point corresponds to 20 ns. The default value is $10 = 200$ ns. The maximum value is $65536 \simeq 1.3$ ms.

2.1.8 Interrupt Delay

F(4/20)A(1) / Base+%42 D16RW

Set the delay time during interrupt input arrival time and actual interrupt generation. 1 point corresponds to 20 ns. The default value is $0 = 0$ ns. The maximum value is $65536 \simeq 1.3$ ms.

2.1.9 Interrupt Source

F(4/20)A(2) / Base+%44 D16W

Choose the interrupt source (1=on, 0=off). 0x03 corresponds to "FIFO Threshold" or "External Input". The default value is 0x03 = "FIFO Threshold".

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FIFO Threshold
External Input
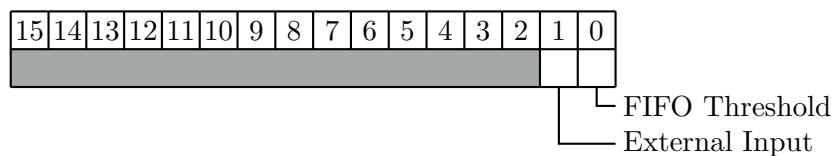
2.1.10 Clock Source

F(6/22)A(0) / Base+%60 D16RW

Choose the time stamp clock source. Default is the external clock.

0 : Internal Clock

1 : External NIM Input 0

2.1.11   Software Veto

F(6/22)A(1) / Base+%62 D16RW

By writing '1' into this register, veto will be on. To clear software veto, write '0'. The default is '0'.

2.1.12   Clear Interrupt

F(9)A(0) / Base+%90 D16R

Clear interrupt signal. In case of VME, this function is invoked by read action.

2.1.13   Reset Time stamp

F(9)A(1) / Base+%92 D16R

Reset the time stamp counter to 0. FIFO memory is also cleared. In case of VME, this function is invoked by read action.

2.1.14   Clear FIFO

F(9)A(2) / Base+%94 D16R

Clear FIFO memory. The time stamp counter is not reset. In case of VME, this function is invoked by read action.

2.1.15   Clear All

F(9)A(3) / Base+%96 D16R

Clear FIFO, interrupt signal, clock scalers. In case of VME, this function is invoked by read action.

2.1.16   Clear Clock

F(9)A(4) / Base+%98 D16R

Clear clock scalers. In case of VME, this function is invoked by read action.

2.1.17   Disable Interrupt

F(24)A(0) / Base+%80 D16W

Disable VME/CAMAC interrupt. In case of VME, this function is invoked by write action. Any write value is acceptable.

2.1.18   Enable Interrupt

F(26)A(0) / Base+%A0 D16W

Enable VME/CAMAC interrupt. In case of VME, this function is invoked by write action. Any write value is acceptable.

2.1.19   Version

F(7)A(0) / Base+%70 D16R

Return the version code of this module. The following is VME Multi Time Stamp Ver 2.0 case.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAMAC/VME				Module ID				Ver **X**.X				Ver X.**X**			
2				7				2				0			

3   Appendix

3.1   Version Information

2.0 16ch version, unified FIFO readout.

1.0 Initial version, 4ch, individual FIFO readout.