LUPO IO & Scaler Firmware
Rev. 1.0

2016 Oct. 11

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1 General

1.1 Function

This firmware enables the functions of the NIM 1ch input/coincidence register, output register, interrupt register and LVDS 16ch scaler.

1.2 Input and coincidence register

The input register returns the logic level of input channels. On the otherhand, the coincidence register returns the coincidence pattern between inputs and the gate signal (NIM Input0). The data is latched by the leading edge of inputs if the gate signal is active. The coindence register is cleared by the clear command or clear input (NIM Input 2).

1.3 Output register

As a output register, NIM outputs ch0–3 can fire pulse and level signals. The width of NIM pulse is variable, and it can be changed 20ns–1.3ms with 20 ns step.

1.4 Interrupt register

As a interrupt register, this module can generete the interrupt signal to VME/CAMAC. The delay time between trigger signal and interrupt generation is variable, and it can be changed 20ns–1.3ms with 20ns step. By the clear command, this interrupt signal is cleared.

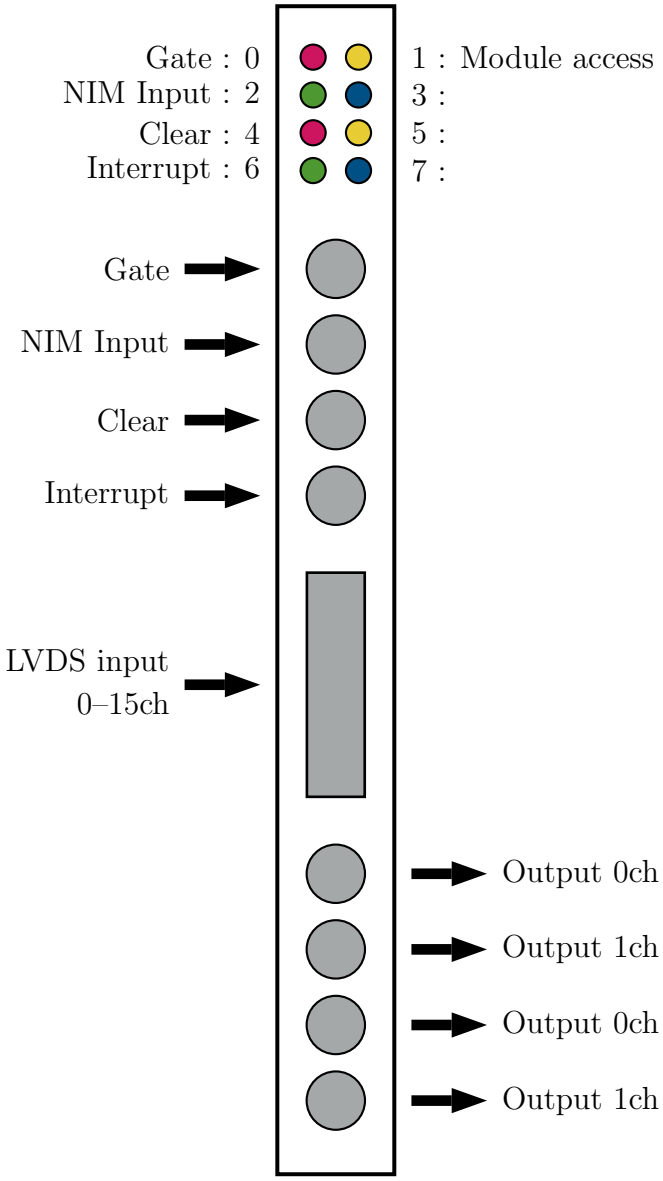
1.5 Input register

There are three types of input register (trigger source, through input, latched input). The trigger source input register is that input pattern is hold by the trigger. The through input is just a condition of trigger logic signals and inputs. The latched input is when trigger logic or input comes, its bit is latched. And it is cleared by clear command.

1.6 Scaler

This firmware has 1ch NIM and 16ch LVDS scaler function. The signals of NIM Input 1 is counted up and can be read. To know the time, three clock scalers of 10MHz, 10KHz, and 1KHz are available.

1.7 Connector



2 Interface

2.1 Register Map

Command list.(Tab.2.1)B

2.1.1 LVDS scaler

F(0–3)A(0–6) / Base+%00–3C D32R

This register return LVDS scaler.

2.1.2 Pulse Width

F(4)A(0) F(20)A(0) / Base+%40 D16RW

Set the pulse width of the output register. 1 point corresponds to 20ns, and default vaule is 10 = 200ns. The maximum value is 65536 $\simeq$ 1.3 ms.

2.1.3 Interrupt Delay

F(4)A(1) F(20)A(1) / Base+%42 D16RW

Set the delay time from trigger generation timing to interrupt generation timing. 1 point corresponds to 20ns, and default vaule is 10 = 200ns. The maximum value is 65536 $\simeq$ 1.3 ms.

2.1.4 Level Output

F(16)A(0) / Base+%00 D16W

Output NIM Level signal. 1=on, 0=off.

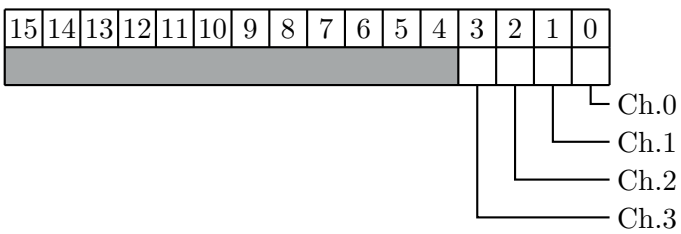


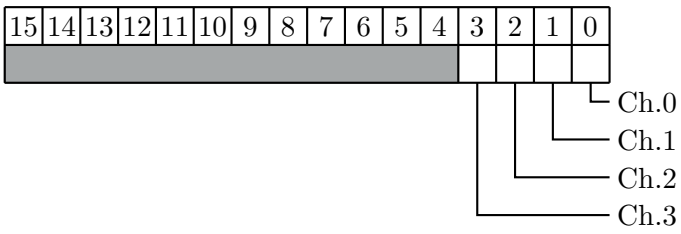
Table 2.1: Register map

CAMAC (R/W)	VME	Register	Data	VME R/W
F(0)A(0)	Base + %00	LVDS Scaler Ch0	D32	read
F(0)A(2)	Base + %04	LVDS Scaler Ch1	D32	read
F(0)A(4)	Base + %08	LVDS Scaler Ch2	D32	read
F(0)A(6)	Base + %0C	LVDS Scaler Ch3	D32	read
F(1)A(0)	Base + %10	LVDS Scaler Ch4	D32	read
F(1)A(2)	Base + %14	LVDS Scaler Ch5	D32	read
F(1)A(4)	Base + %18	LVDS Scaler Ch6	D32	read
F(1)A(6)	Base + %1C	LVDS Scaler Ch7	D32	read
F(2)A(0)	Base + %20	LVDS Scaler Ch8	D32	read
F(2)A(2)	Base + %24	LVDS Scaler Ch9	D32	read
F(2)A(4)	Base + %28	LVDS Scaler Ch10	D32	read
F(2)A(6)	Base + %2C	LVDS Scaler Ch11	D32	read
F(3)A(0)	Base + %30	LVDS Scaler Ch12	D32	read
F(3)A(2)	Base + %34	LVDS Scaler Ch13	D32	read
F(3)A(4)	Base + %38	LVDS Scaler Ch14	D32	read
F(3)A(6)	Base + %3C	LVDS Scaler Ch15	D16	read
F(16)A(0)	Base + %00	Level Output	D16	write
F(17)A(0)	Base + %10	Pulse Output	D16	write
F(4)A(0) F(20)A(0)	Base + %40	Pulse Width	D16	read/write
F(4)A(1) F(20)A(1)	Base + %42	Interrupt Delay	D16	read/write
F(4)A(4) F(20)A(4)	Base + %48	Scaler VETO	D16	read/write
F(5)A(0)	Base + %50	NIM Input	D16	read
F(5)A(1)	Base + %52	NIM Coincidence	D16	read
F(6)A(0)	Base + %60	Clock 10MHz	D32	read
F(6)A(2)	Base + %64	Clock 10KHz	D32	read
F(6)A(4)	Base + %68	Clock 1KHz	D32	read
F(6)A(6)	Base + %6C	Scalr NIM Input	D32	read
F(7)A(0)	Base + %70	Version	D16	read
F(9)A(0)	Base + %90	Clear data and interrupt	D16	read
F(9)A(1)	Base + %92	Clear all	D16	read
F(24)A(0)	Base + %80	Disable Interrupt	D16	write
F(26)A(0)	Base + %A0	Enable Interrupt	D16	write

2.1.5 Pulse Output

F(17)A(0) / Base+%10 D16W

Output NIM pulse with given width.



2.1.6 Clear Register

F(9)A(0) / Base+%90 D16R Clear interrupt and coincidence register. VME case, this register is read access.

2.1.7 Clear All Register

F(9)A(1) / Base+%92 D16R Clear interrupt, coincidence and all scaler values. VME case, this register is read access.

2.1.8 Disable Interrupt

F(24)A(0) / Base+%80 D16W Disable VME/CAMAC interrupt. VME case, this register is write access.

2.1.9 Enable Interrupt

F(26)A(0) / Base+%A0 D16W Enable VME/CAMAC interrupt. VME case, this register is write access.

2.1.10 Version

Reteruns version code of this module. Followind is VME IO Scaler Rev 1.0:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAMAC/VME				Module ID				Rev **X**.X				Rev X.**X**			
2				B				1				0			

3 Appendix

3.1 Version Information

1.4 Clock and NIM scalers are implemented

1.2 Version code is added

1.1 Swapped gate input and NIM input

1.0 First version