LUPO DAQ Master Module
Rev. 1.6

2018 Apr. 19

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1 General

1.1 Function

1.2 Output register

As a output register, NIM outputs ch0–1 can fire pulse and level signals. The width of NIM pulse is variable, and it can be changed 20ns–1.3ms with 20 ns step.

1.3 Interrupt register

As a interrupt register, this module can generate the interrupt signal to VME/CAMAC. The delay time between trigger signal and interrupt generation is variable, and it can be changed 20ns–1.3ms with 20ns step. By the clear command, this interrupt signal is cleared.

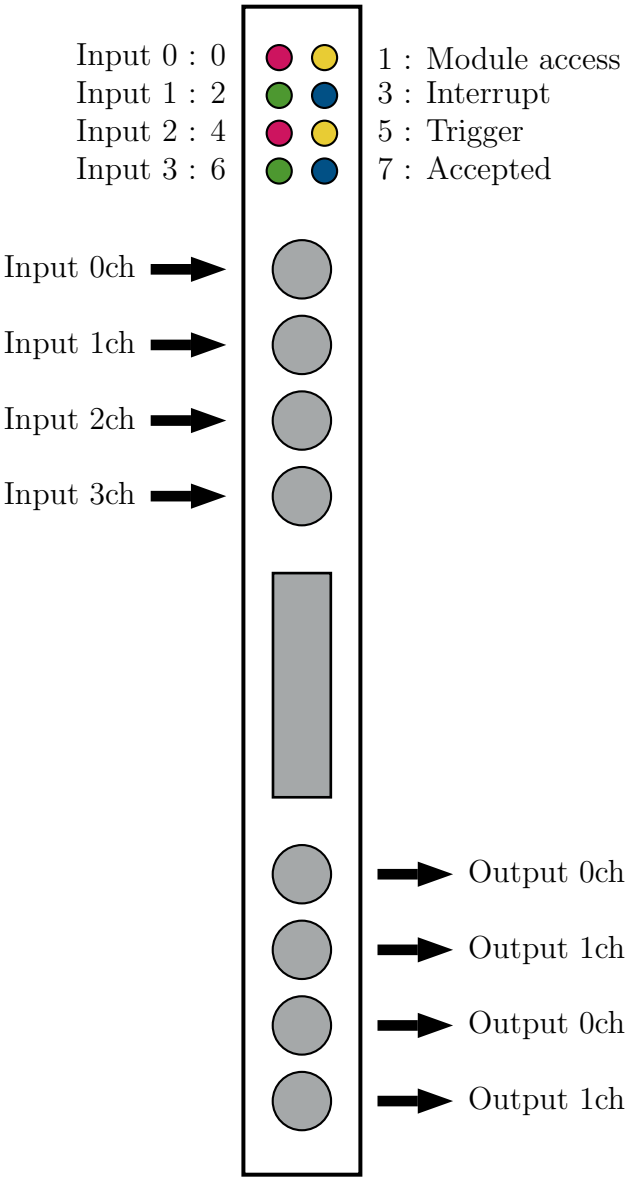
1.4 Input register

There are three types of input register (trigger source, through input, latched input). The trigger source input register is that input pattern is hold by the trigger. The through input is just a condition of trigger logic signals and inputs. The latched input is when trigger logic or input comes, its bit is latched. And it is cleared by clear command.

1.5 Scaler

There are several types of scaler (counter) registers. Scaler 0–3ch are the counter of input channel 0–3ch. Internal ungated and gated triggers could be obtained. Clock 1, 10K, 1KHz are the internal clock counters. Clock 10KHz Aux is a special clock counter of 10KHz. The clear function or Aux Scaler is independent of other scalers. The read access of Clear all scaler clean up all scaler values except for this Aux Scaler. To clear the Aux Scaler, read access of Clear Aux Scaler or Clear All is required.

1.6 Connector


Input 0 : 0
Input 1 : 2
Input 2 : 4
Input 3 : 6
1 : Module access
3 : Interrupt
5 : Trigger
7 : Accepted
Input 0ch
Input 1ch
Input 2ch
Input 3ch
Output 0ch
Output 1ch
Output 0ch
Output 1ch

2 Interface

2.1 Register Map

Command list.(Tab.2.1).

2.1.1 Pulse Width

F(4)A(0) F(20)A(0) / Base+%40 D16RW

Set the pulse width of the output register. 1 point corresponds to 20ns, and default value is 10 = 200ns. The maximum value is 65536 $\simeq$ 1.3 ms.

2.1.2 Interrupt Delay

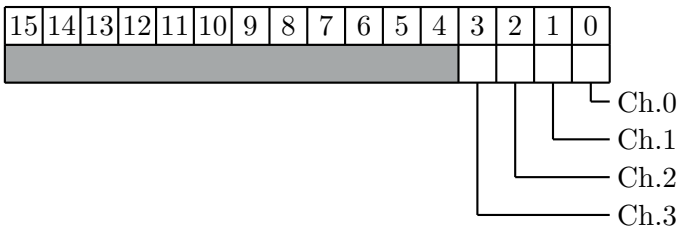
F(4)A(1) F(20)A(1) / Base+%42 D16RW

Set the delay time from trigger generation timing to interrupt generation timing. 1 point corresponds to 20ns, and default value is 10 = 200ns. The maximum value is 65536 $\simeq$ 1.3 ms.

2.1.3 Level Output

F(16)A(0) / Base+%00 D16W

Output NIM Level signal. 1=on, 0=off.



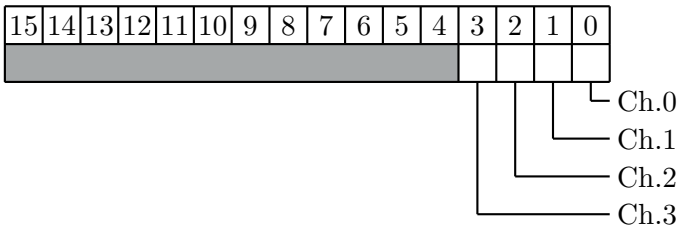
2.1.4 Pulse Output

F(17)A(0) / Base+%10 D16W

Output NIM pulse with given width.

Table 2.1: Register map

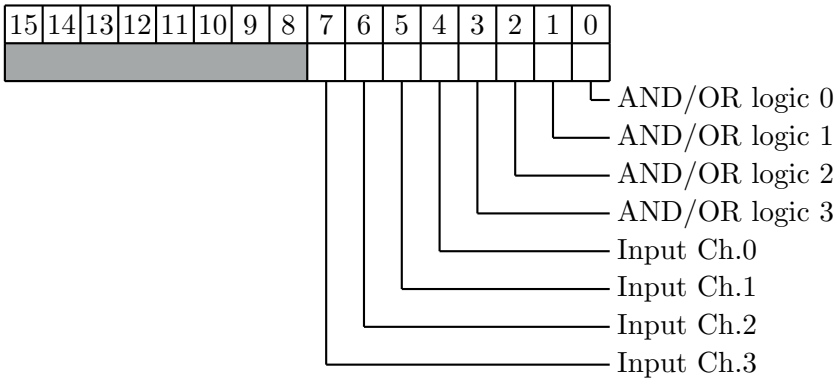
CAMAC (R/W)		VME	Register	Data	VME R/W
F(0)A(0)		Base + %00	Clock 1MHz	D32	read
F(0)A(2)		Base + %04	Clock 10KHz	D32	read
F(0)A(4)		Base + %08	Clock 1KHz	D32	read
F(0)A(6)		Base + %0c	Clock 10KHz Aux	D32	read
	F(16)A(0)	Base + %00	Level Output	D16	write
	F(17)A(0)	Base + %10	Pulse Output	D16	write
F(1)A(0)		Base + %10	Ungated trigger	D32	read
F(1)A(2)		Base + %14	Gated trigger	D32	read
F(2)A(0)		Base + %20	Scaler 0ch	D32	read
F(2)A(2)		Base + %24	Scaler 1ch	D32	read
F(2)A(4)		Base + %28	Scaler 2ch	D32	read
F(2)A(8)		Base + %2c	Scaler 3ch	D32	read
F(3)A(0)		Base + %30	Trigger source	D16	read
F(3)A(1)		Base + %32	Through input	D16	read
F(3)A(2)		Base + %34	Latch input	D16	read
F(4)A(0)	F(20)A(0)	Base + %40	Pulse Width	D16	read/write
F(4)A(1)	F(20)A(1)	Base + %42	Interrupt Delay	D16	read/write
F(4)A(3)	F(20)A(3)	Base + %46	Delay logic Delay	D16	read/write
F(4)A(4)	F(20)A(4)	Base + %48	Delay logic Source	D16	read/write
F(4)A(5)	F(20)A(5)	Base + %4a	Delay logic Clear	D16	read/write
F(5)A(0)	F(21)A(0)	Base + %50	Output 0ch Config	D16	read/write
F(5)A(1)	F(21)A(1)	Base + %52	Output 1ch Config	D16	read/write
F(5)A(2)	F(21)A(2)	Base + %54	Output 2ch Config	D16	read/write
F(5)A(3)	F(21)A(3)	Base + %56	Output 3ch Config	D16	read/write
F(6)A(0)	F(22)A(0)	Base + %60	AND/OR Register 0	D16	read/write
F(6)A(1)	F(22)A(1)	Base + %62	AND/OR Register 1	D16	read/write
F(6)A(2)	F(22)A(2)	Base + %64	AND/OR Register 2	D16	read/write
F(6)A(3)	F(22)A(3)	Base + %66	AND/OR Register 3	D16	read/write
F(6)A(4)	F(22)A(4)	Base + %68	Trigger Configuration	D16	read/write
F(6)A(5)	F(22)A(5)	Base + %6a	Trigger Activation	D16	read/write
F(7)A(0)		Base + %70	Version	D16	read
F(9)A(0)		Base + %90	Clear interrupt & busy	D16	read
F(9)A(1)		Base + %92	Clear all scaler	D16	read
F(9)A(2)		Base + %94	Clear trigger scaler	D16	read
F(9)A(3)		Base + %96	Clear all	D16	read
F(9)A(4)		Base + %98	Clear Aux Scaler	D16	read
F(9)A(5)		Base + %9a	Delay Logic Soft Clear	D16	read
	F(24)A(0)	Base + %80	Disable Interrupt	D16	write
	F(26)A(0)	Base + %A0	Enable Interrupt	D16	write



2.1.5 Trigger source

F(3)A(0) / Base+%30 D16R

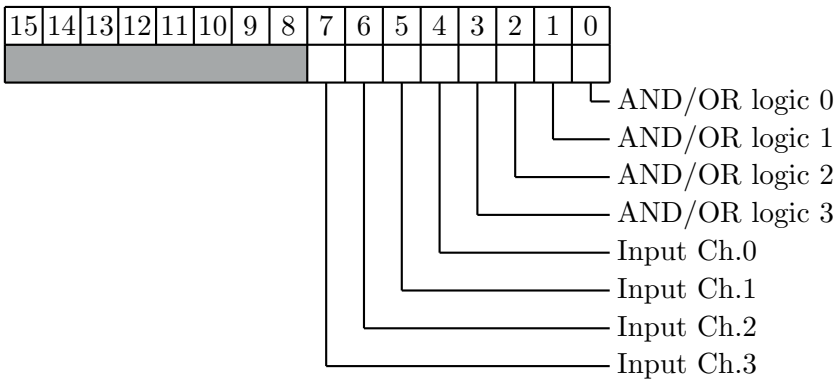
This register returns the hit pattern of AND/OR Logic and Input channels. The hit pattern is latched by the trigger timing. This register can be used as the coincidence/input register. By accessing the Clear interrupt or Clear all register, this register is cleared.



2.1.6 Through input

F(3)A(1) / Base+%32 D16R

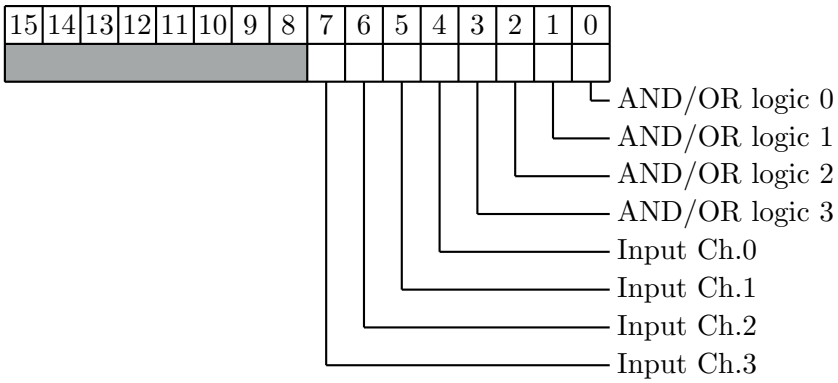
This register returns the current hit pattern of AND/OR Logic and Input channels.



2.1.7 Latch input

F(3)A(0) / Base+%34 D16R

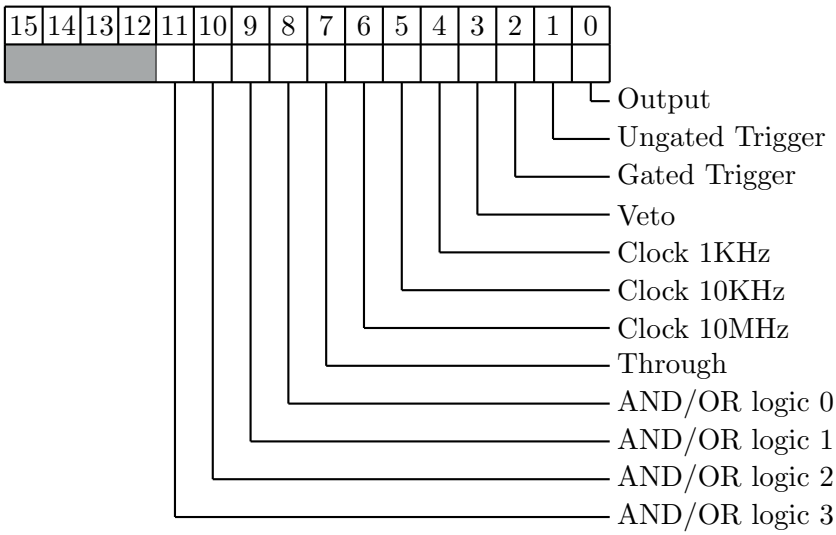
This register returns the hit pattern of AND/OR Logic and Input channels. The hit pattern is hold when input comes. By accessing the Clear interrupt or Clear all register, this register is cleared.



2.1.8 Output Configuration 0–3

F(5)A(0–3) F(21)A(0–3) / Base+%50–56 D16RW

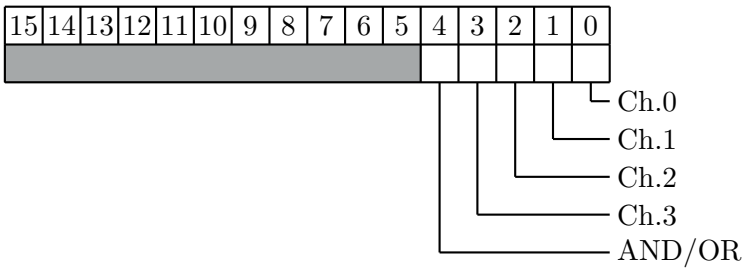
Configure NIM output channels. You can select the output channel as Ungated (Generated) Trigger, Gated (Accepted) Trigger, VETO, and output register. From rev1.4, AND/OR logic 0–3 can be output. Usually, you should on only 1 bit, if multiple bits are on, output will be OR of these. As a output register case, Output Config. 0 will be Output Reg. 0, Output Config 1 will be Output Reg. 1 . The default values are: Ch.0 = “0001”ACh.1 = “0001”ACh.2 = “0010”ACh.3 = “0100”(Ch.0 and 1 are as the Output Reg. Ch.2 is Ungated Trigger, Ch.3 is Gated Trigger.)



2.1.9 AND/OR Logic 0–3

F(6)A(0–3) F(22)A(0–3) / Base+%60–66 D16RW

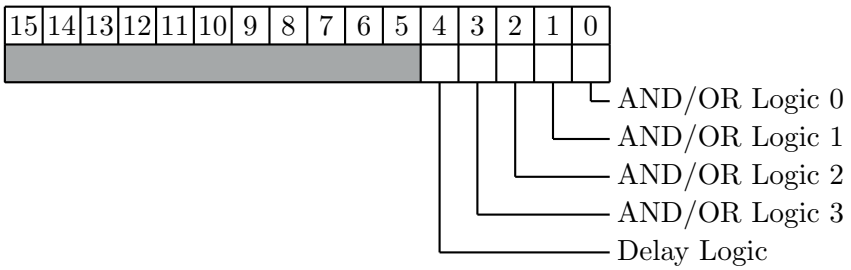
Register AND/OR logic to define the trigger. By setting these AND/OR logic to Trigger Register, the configuration of the trigger generation is determined. 4th bit corresponds to AND(=1) / OR(=0). For example, “10011” means that register logical AND or Ch0 and Ch1. “01001” case, it is logical OR of Ch0 and Ch3. The default values are: lo0 = “00001”Alo1 = “00010”Alo2 = “00100”Alo3 = “01000”.



2.1.10 Trigger Configuration

F(6)A(4) F(22)A(4) / Base+%68 D16RW

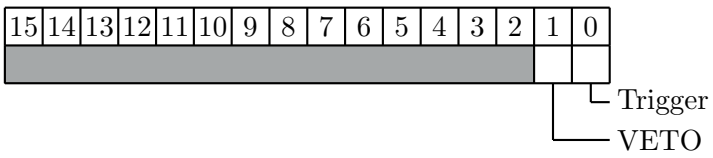
Select AND/OR logic as the trigger source. This case, trigger will be OR of selected bits. The default value is ”0001”.



2.1.11 Trigger Activation

F(6)A(5) F(22)A(5) / Base+%6a D16RW

The validation of trigger and VETO. (1=On, 0=Off) ’01’(=1) is used to check the trigger. ’11’(=3) is DAQ start case. ’00’(=0) or ’10’(=2) cases, ungated trigger isn’t generated. The default value is ’01’(=1).



2.1.12 Delay Logic Delay time

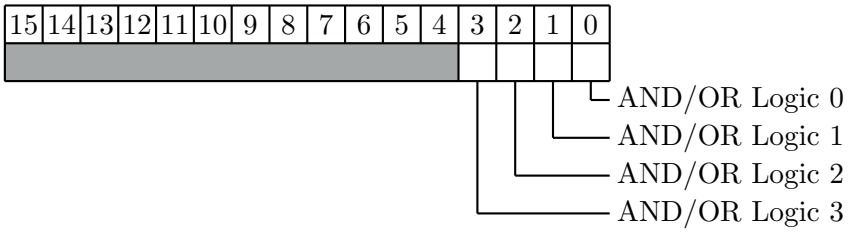
F(4)A(3) F(20)A(3) / Base+%46 D16RW

Set the delay time from the delay logic. 1 point corresponds to 20ns, and default value is 100 = 2000ns. The maximum value is 65536 $\simeq$ 1.3 ms.

2.1.13 Delay Logic source

F(4)A(4) F(20)A(4) / Base+%48 D16RW

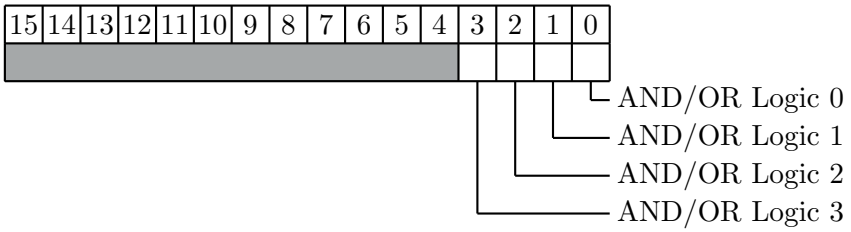
Choose AND/OR logic as the delay logic source. Source signal will be OR of selected bits. The default value is "0000" (disable).



2.1.14 Delay Logic clear

F(4)A(5) F(20)A(5) / Base+%4a D16RW

Choose AND/OR logic for the delay logic clear. Source signal will be OR of selected bits. The default value is "0000" (disable).



2.1.15 Clear Aux Scaler

F(9)A(4) / Base+%98 D16R

Clear 10KHz Aux scaler only. VME case, this register is read access.

2.1.16 Delay logic soft clear

F(9)A(5) / Base+%9a D16R

Software clear for delay logic function.

2.1.17 Disable Interrupt

Disable VME/CAMAC interrupt. VME case, this register is write access.

2.1.18 Enable Interrupt

Enable VME/CAMAC interrupt. VME case, this register is write access.

2.1.19 Version

Returns version code of this module. Following is VME DAQ Master Rev 1.6:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAMAC/VME				Module ID				Rev **X**.X				Rev X.**X**			
2				9				1				6			

3 Appendix

3.1 Version Information

1.6 Delay logic function is added

1.5 AND/OR logic can output from NIM Output

1.4 Bug fix for Scaler3 readout

1.3 Aux Scaler is implemented.

1.2 Through input and latch input are implemented.

1.1 Interrupt function is fixed. The trigger source register in available. Clocks and through signals are available on the output configuration.

1.0 First version