LUPO DAQ Master Module
Rev. 1.1

2010 Aug. 30

1 General

1.1 Function

1.2 Output register

As a output register, NIM outputs ch0–1 can fire pulse and level signals. The width of NIM pulse is variable, and it can be changed 20ns–1.3ms with 20 ns step.

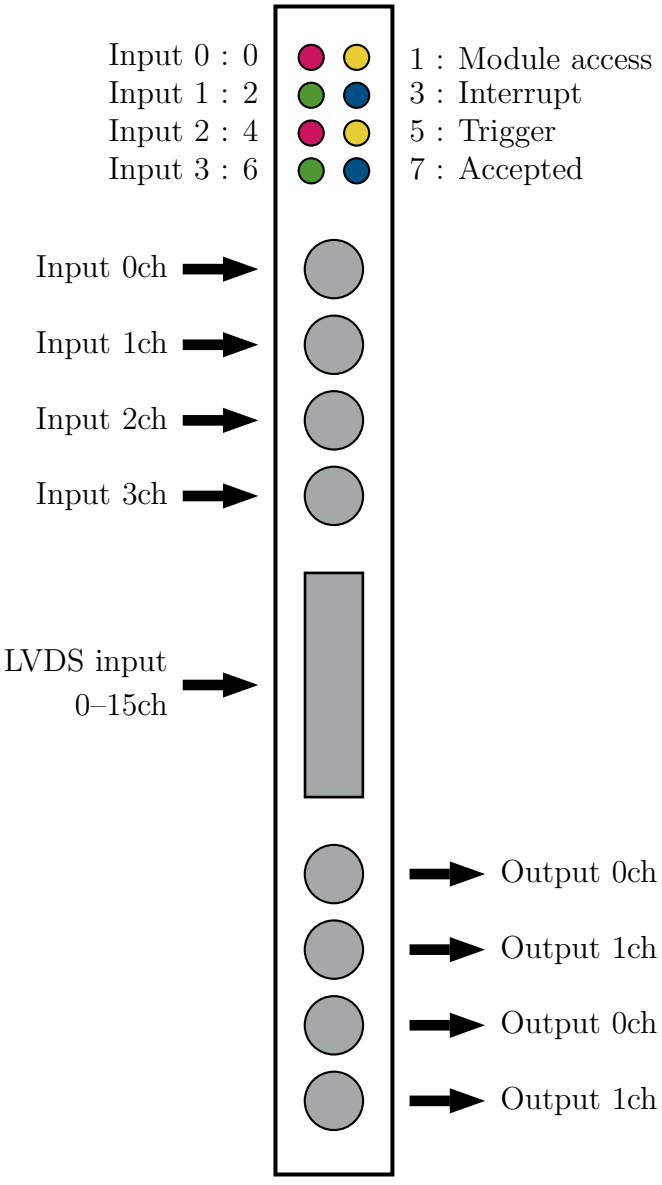
1.3 Interrupt register

As a interrupt register, this module can generete the interrupt signal to VME/CAMAC. The delay time between trigger signal and interrupt generation is variable, and it can be changed 20ns–1.3ms with 20ns step. By the clear command, this interrupt signal is cleared.

1.4 Trigger generator

This module can generate the trigger signal according to registerd trigger logic. The VETO signal which corresponds to DAQ (computer) busy is also generated. The trigger is inhibited by VETO within inside of LUPO.

1.5 Connector


Input 0 : 0
Input 1 : 2
Input 2 : 4
Input 3 : 6
1 : Module access
3 : Interrupt
5 : Trigger
7 : Accepted
Input 0ch
Input 1ch
Input 2ch
Input 3ch
LVDS input
0–15ch
Output 0ch
Output 1ch
Output 0ch
Output 1ch

2 Interface

2.1 Register Map

Command list.(Tab.2.1)。

2.1.1 Pulse Width

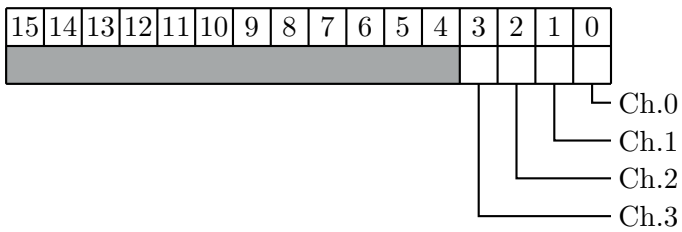
Set the pulse width of the output register. 1 point corresponds to 20ns, and default vaule is 10 = 200ns. The maximum value is 65536 $\simeq$ 1.3 ms.

2.1.2 Interrupt Delay

Set the delay time from trigger generation timing to interrupt generation timing. 1 point corresponds to 20ns, and default vaule is 10 = 200ns. The maximum value is 65536 $\simeq$ 1.3 ms.

2.1.3 Level Output

Output NIM Level signal. 1=on, 0=off.

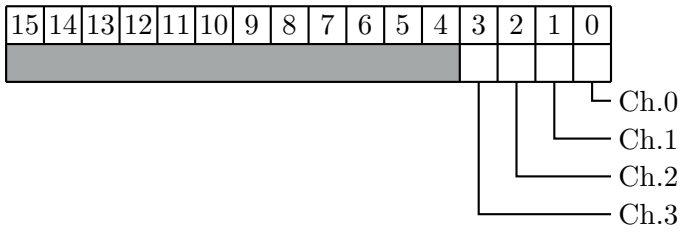


2.1.4 Pulse Output

F(17)A(0) / Base+%10 D16W Output NIM pulse with given width.

Table 2.1: Register map

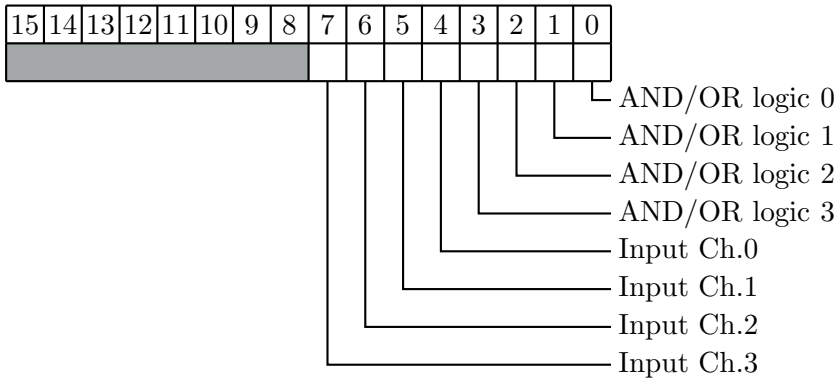
CAMAC (R/W)	VME	Register	Data	VME R/W
F(0)A(0)	Base + %00	Clock 1MHz	D32	read
F(0)A(2)	Base + %04	Clock 10KHz	D32	read
F(0)A(4)	Base + %08	Clock 1KHz	D32	read
F(16)A(0)	Base + %00	Level Output	D16	write
F(17)A(0)	Base + %10	Pulse Output	D16	write
F(1)A(0)	Base + %10	Ungated trigger	D32	read
F(1)A(2)	Base + %14	Gated trigger	D32	read
F(2)A(0)	Base + %20	Scaler 0ch	D32	read
F(2)A(2)	Base + %24	Scaler 1ch	D32	read
F(2)A(4)	Base + %28	Scaler 2ch	D32	read
F(2)A(8)	Base + %2c	Scaler 3ch	D32	read
F(3)A(0)	Base + %30	Trigger Source	D16	read
F(4)A(0) F(20)A(0)	Base + %40	Pulse Width	D16	read/write
F(4)A(1) F(20)A(1)	Base + %42	Interrupt Delay	D16	read/write
F(5)A(0) F(21)A(0)	Base + %50	Output 0ch Config	D16	read/write
F(5)A(1) F(21)A(1)	Base + %52	Output 1ch Config	D16	read/write
F(5)A(2) F(21)A(2)	Base + %54	Output 2ch Config	D16	read/write
F(5)A(3) F(21)A(3)	Base + %56	Output 3ch Config	D16	read/write
F(6)A(0) F(22)A(0)	Base + %60	AND/OR Register 0	D16	read/write
F(6)A(1) F(22)A(1)	Base + %62	AND/OR Register 1	D16	read/write
F(6)A(2) F(22)A(2)	Base + %64	AND/OR Register 2	D16	read/write
F(6)A(3) F(22)A(3)	Base + %66	AND/OR Register 3	D16	read/write
F(6)A(4) F(22)A(4)	Base + %68	Trigger Configuration	D16	read/write
F(6)A(5) F(22)A(5)	Base + %6a	Trigger Activation	D16	read/write
F(7)A(0)	Base + %70	Version	D16	read
F(9)A(0)	Base + %90	Clear intterupt & busy	D16	read
F(9)A(1)	Base + %92	Clear all scaler	D16	read
F(9)A(2)	Base + %94	Clear trigger scaler	D16	read
F(9)A(3)	Base + %96	Clear all	D16	read
F(24)A(0)	Base + %80	Disable Interrupt	D16	write
F(26)A(0)	Base + %A0	Enable Interrupt	D16	write



2.1.5 Trigger source

F(3)A(0) / Base+%30 D16R

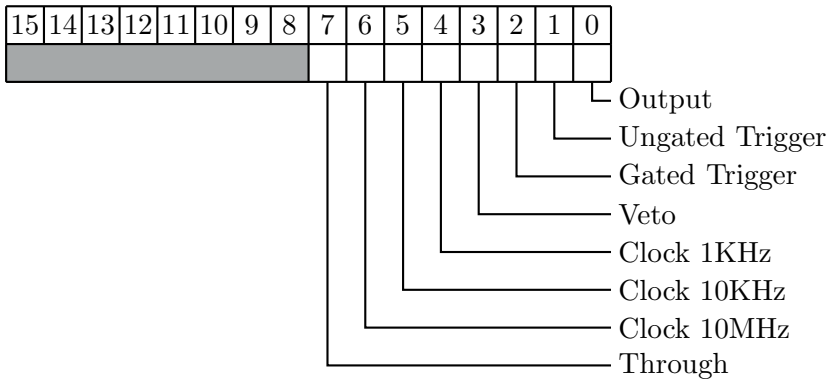
This register returns the hit pattern of AND/OR Logic and Input channels. The hit pattern is latched by the trigger timing. This register can be used as the coincidence/input register. By accessing the Clear intterupt or Clear all register, this register is cleared.



2.1.6 Output Configuration 0–3

F(5)A(0–3) F(21)A(0–3) / Base+%50–56 D16RW

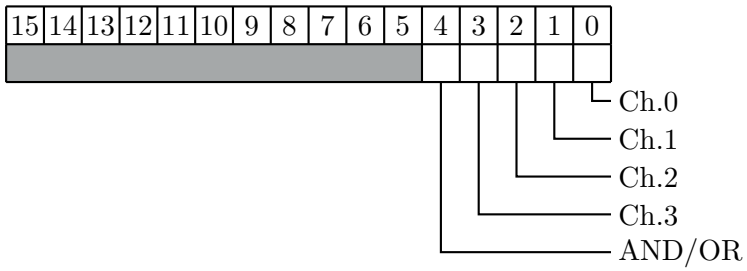
Configure NIM output channels. You can select the output channel as Ungated (Generated) Trigger, Gated (Accepted) Trigger, VETO, and output register. Usually, you should on only 1 bit, if multiple bits are on, output will be OR of these. As a output register case, Output Config. 0 will be Output Reg. 0, Output Config 1 will be Output Reg. 1 になります。The default values are: Ch.0 = “0001”、Ch.1 = “0001”、Ch.2 = “0010”、Ch.3 = “0100”(Ch.0 and 1 are as the Output Reg. Ch.2 is Ungated Trigger, Ch.3 is Gated Trigger.)



2.1.7 AND/OR Logic 0–3

F(6)A(0–3) F(22)A(0–3) / Base+%60–66 D16RW

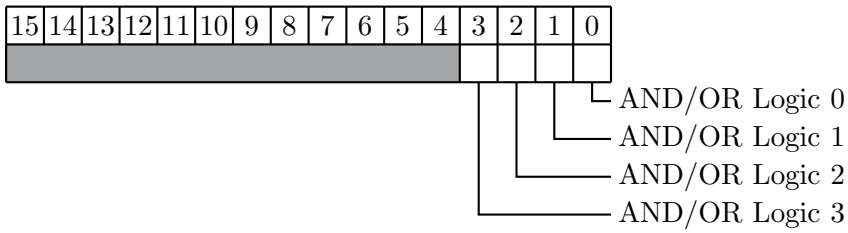
Register AND/OR logic to define the trigger. By setting these AND/OR logic to Trigger Register, the configuration of the trigger generation is determined. 4th bit corresponds to AND(=1) / OR(=0). For example, “10011” means that register logical AND or Ch0 and Ch1. “01001” case, it is logical OR of Ch0 and Ch3. The default values are: lo0 = “00001”、lo1 = “00010”、lo2 = “00100”、lo3 = “01000”.



2.1.8 Trigger Register

F(6)A(4) F(22)A(4) / Base+%68 D16RW

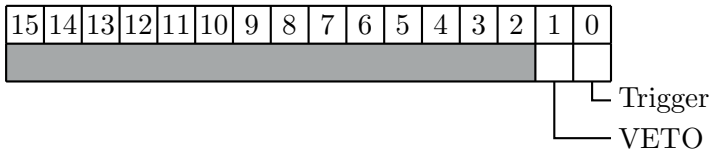
Select AND/OR logic as the trigger source. This case, trigger will be OR of selected bits. The default value is ”0001”.



2.1.9 Trigger Activation

F(6)A(5) F(22)A(5) / Base+%6a D16RW

The validation of tirgger and VETO. (1=On, 0=Off) '01'(=1) is used to check the trigger. '11'(=3) is DAQ start case. '00'(=0) or '10'(=2) cases, ungated trigger isn't generated. The default value is '01'(=1).



2.1.10 Clear Register

Clear interrupt register. VME case, this register is read access.

2.1.11 Disable Interrupt

Disable VME/CAMAC interrupt. VME case, this register is write access.

2.1.12 Enable Interrupt

Enable VME/CAMAC interrupt. VME case, this register is write access. VME/CAMAC 割り込みを許可します。

2.1.13 Version

Reteruns version code of this module. Followind is CAMAC DAQ Master Rev 1.0:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAMAC/VME				Module ID				Rev **X**.X				Rev X.**X**			
1				9				1				0			

3 Appendix

3.1 Version Information

1.1 Interrupt function is fixed. The trigger source register in available. Clocks and through signals are available on the output configuration.

1.0 First version