

FPGA Lecture for LUPO and GTO

Vol.3

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Important options

Right click "Synthesize" -> Properties

Switch Name	Property Name	Value
-opt_mode	Optimization Goal	Speed
-opt_level	Optimization Effort	Normal
-iuc	Use Synthesis Constraints File	<input checked="" type="checkbox"/>
-uc	Synthesis Constraints File	...
-lso	Library Search Order	...
-keep_hierarchy	Keep Hierarchy	Yes
-netlist_hierarchy	Netlist Hierarchy	As Optimized
-write_timing_constraints	Write Timing Constraints	<input type="checkbox"/>
-cross_clock_analysis	Cross Clock Analysis	<input type="checkbox"/>
-hierarchy_separator	Hierarchy Separator	/
-bus_delimiter	Bus Delimiter	<>

Many cases, "Keep Hierarchy" is useful (sometimes, ineffective modules are merged with other components)

Right click "Implement Design" -> Properties

Switch Name	Property Name	Value
-timing	Perform Timing-Driven Packing and Placement	<input type="checkbox"/>
-ol	Map Effort Level	High
-xe	Extra Effort	None
-t	Starting Placer Cost Table (1-100)	1
-logic_opt	Combinatorial Logic Optimization	<input type="checkbox"/>
-register_duplication	Register Duplication	Off
-x	Ignore User Timing Constraints	<input type="checkbox"/>
-ntd	Timing Mode	Non Timing Driven
-u	Trim Unconnected Signals	<input checked="" type="checkbox"/>

Sometimes, "Trim Unconnected Signals" makes problem (if you have problems let's disable this option)



Simulation with Delay 1/3

We can simulate the delay of components and wires in FPGA

Right click "Implement Design" -> Properties

Switch Name	Property Name	Value
	Simulation Model Target	VHDL
-s	Device Speed Grade/Select ABS Minimum	-4
-fn	Retain Hierarchy	<input type="checkbox"/>
-mhf	Generate Multiple Hierarchical Netlist Files	<input checked="" type="checkbox"/>
-tp	Bring Out Global Tristate Net as a Port	<input type="checkbox"/>
	Global Tristate Port Name	GTS_PORT
-gp	Bring Out Global Set/Reset Net as a Port	<input type="checkbox"/>
	Global Set/Reset Port Name	GSR_PORT
-tb	Generate Testbench File	<input type="checkbox"/>
-ti	Rename Design Instance in Testbench File to	UUT
-insert_pp_buffers	Insert Buffers to Prevent Pulse Swallowing	<input checked="" type="checkbox"/>
	Other NETGEN Command Line Options	
-tm	Rename Top Level Entity to	Structure
-ar	Rename Top Level Architecture To	
-tpw	Tristate On Configuration Pulse Width	
-rpw	Reset On Configuration Pulse Width	100
-a	Generate Architecture Only (No Entity Declaration)	<input type="checkbox"/>
-extid	Output Extended Identifiers	<input type="checkbox"/>
-tm	Rename Top Level Module To	
-ul	Include 'uselib Directive in Verilog File	<input type="checkbox"/>
-sdf_anno	Include sdf_annotate task in Verilog File	<input checked="" type="checkbox"/>
-sdf_path	Path Used in sdf_annotate task	Default
-ne	Do Not Escape Signal and Instance Names in Netlist	<input type="checkbox"/>
-ism	Include SIMPRIM Models in Verilog File	<input type="checkbox"/>
-insert_glbl	Automatically Insert glbl Module in the Netlist	<input checked="" type="checkbox"/>

```
26 -- simulation
27 -----
28 LIBRARY ieee;
29 USE ieee.std_l
30
31 -- Uncomment t
32 -- arithmetic
33 --USE ieee.nun
34
35 ENTITY dtest4;
36 END dtest4;
37
38 ARCHITECTURE t
39
40 -- Compon
41
42 COMPONENT
43 PORT (
44     CLOCK
45     LED :
46     NIN :
47     NOUT
48     XRX :
49     XTX :
50 );
51 END COMPON
52
53
54 --Inputs
55 signal CLOCK
56 signal NIN
57 signal XRX
58
59 --Outputs
60 signal LED
61 signal NOUT
62 signal XTX
63
64 -- Clock pe
65 constant CI
66
67 BEGIN
68
69 -- Instantia
70 uut: DLGTO
71     CLOCK
```

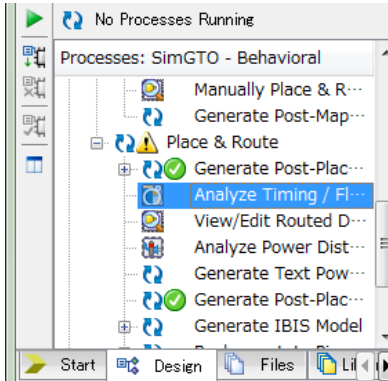
Generate Post-Place & Route Simulation Model



Simulation with Delay 3/3

Change the delay by moving components in FPGA. (example is LUT1)

```
library UNISIM;  
use UNISIM.VComponents.all;  
  
entity THR is  
    Port ( s : in  STD_LOGIC;  
          q : out  STD_LOGIC);  
end THR;  
  
architecture Behavioral of THR is  
  
begin  
  
    LUT1_inst : LUT1  
        generic map (  
            INIT => "10")  
        port map (  
            0 => q,  
            I0 => s  
        );  
  
end Behavioral;
```



Launch PlanAhead

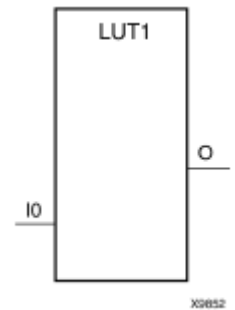
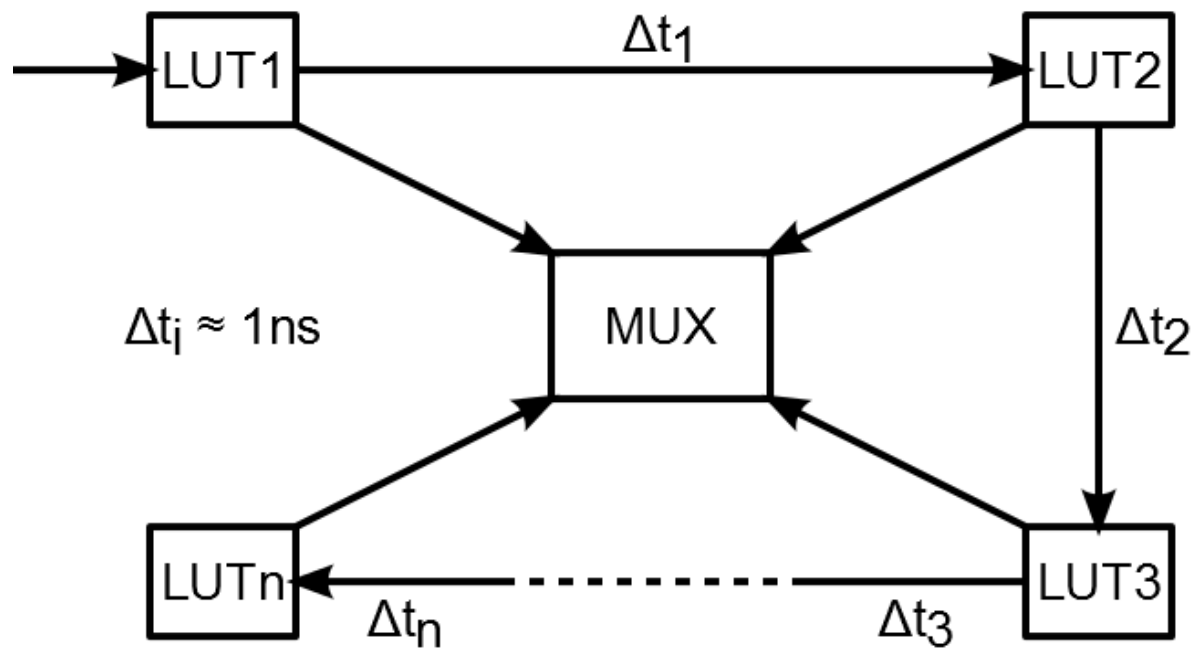
You can move by mouse drag

You can fix the component, and automatically written in UCF

```
# PlanAhead Generated physical constraints  
INST "THRI2/LUT1_inst" BEL = F;  
INST "THRI2/LUT1_inst" LOC = SLICE_X30Y33;
```

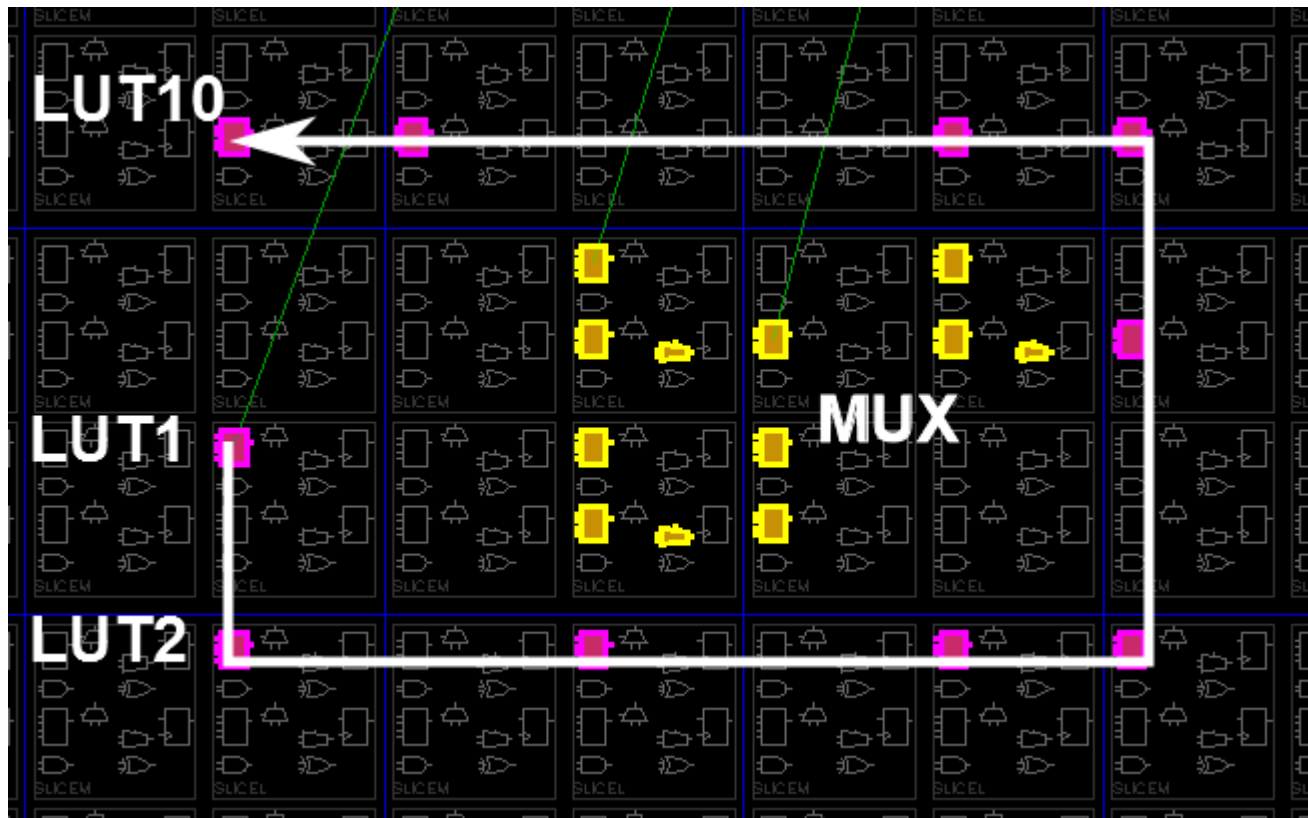


Logic delay by wiring 1/3



Logic delay by wiring 2/3

By floor planner



Logic delay by wiring 3/3

Example of UCF file

```
INST "Inst_delay2/LUT1_inst" BEL = G;  
INST "Inst_delay2/LUT1_inst" LOC = SLICE_X7Y8;  
INST "Inst_delay2/LUT2_inst" BEL = G;  
INST "Inst_delay2/LUT2_inst" LOC = SLICE_X7Y7;  
INST "Inst_delay2/LUT3_inst" BEL = G;  
INST "Inst_delay2/LUT3_inst" LOC = SLICE_X9Y7;  
INST "Inst_delay2/LUT4_inst" BEL = G;  
INST "Inst_delay2/LUT4_inst" LOC = SLICE_X11Y7;  
INST "Inst_delay2/LUT5_inst" BEL = G;  
INST "Inst_delay2/LUT5_inst" LOC = SLICE_X12Y7;  
INST "Inst_delay2/LUT6_inst" BEL = F;  
INST "Inst_delay2/LUT6_inst" LOC = SLICE_X12Y9;  
INST "Inst_delay2/LUT7_inst" BEL = F;  
INST "Inst_delay2/LUT7_inst" LOC = SLICE_X12Y10;  
INST "Inst_delay2/LUT8_inst" BEL = F;  
INST "Inst_delay2/LUT8_inst" LOC = SLICE_X11Y10;  
INST "Inst_delay2/LUT9_inst" BEL = F;  
INST "Inst_delay2/LUT9_inst" LOC = SLICE_X8Y10;  
INST "Inst_delay2/LUT10_inst" BEL = F;  
INST "Inst_delay2/LUT10_inst" LOC = SLICE_X7Y10;
```

Some times, multiple LUTs packed into 1LUT.

To avoid this, hand-write constraints are required before floor planner.

