FPGA Lecture for LUPO and GTO

Vol.3

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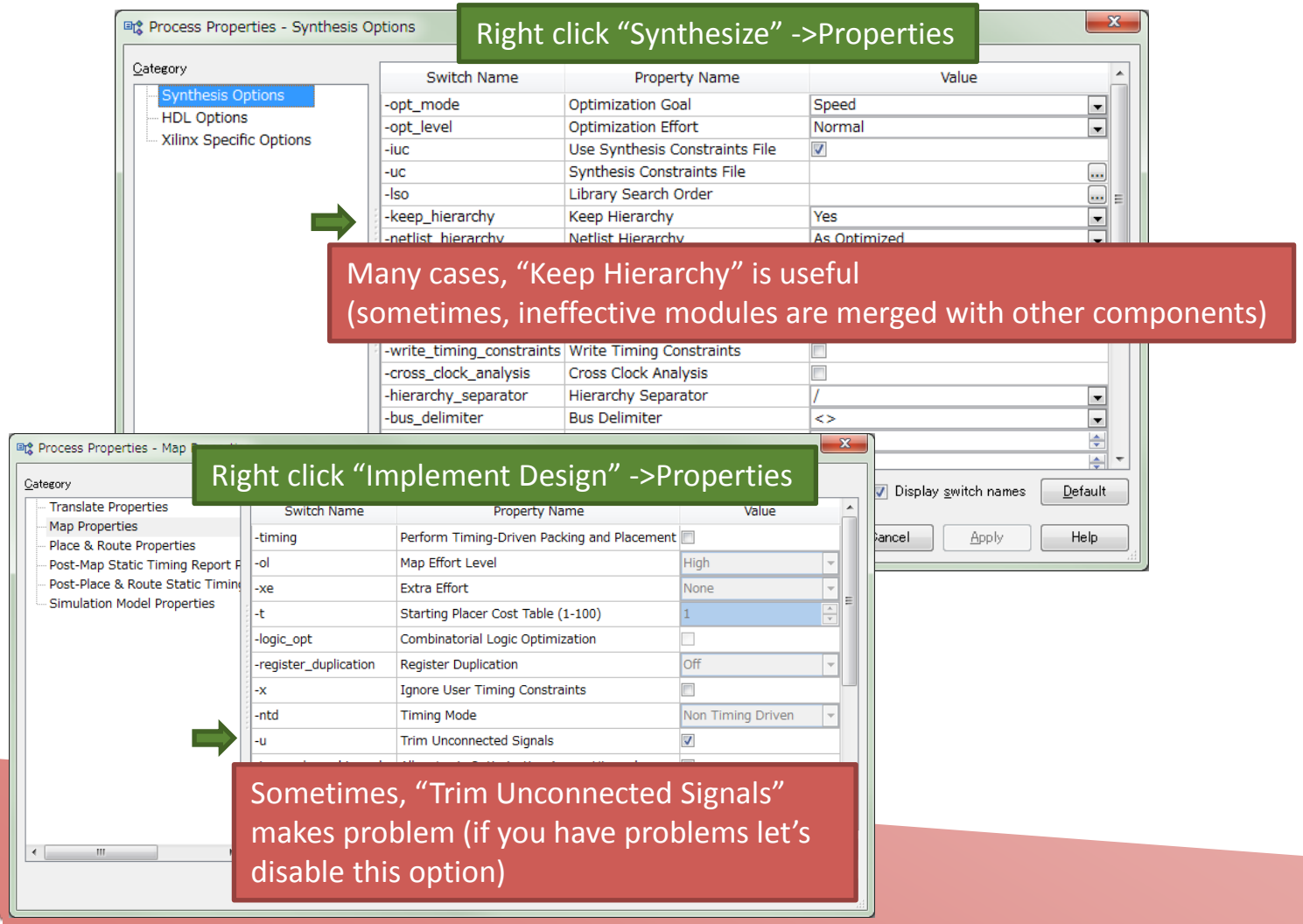
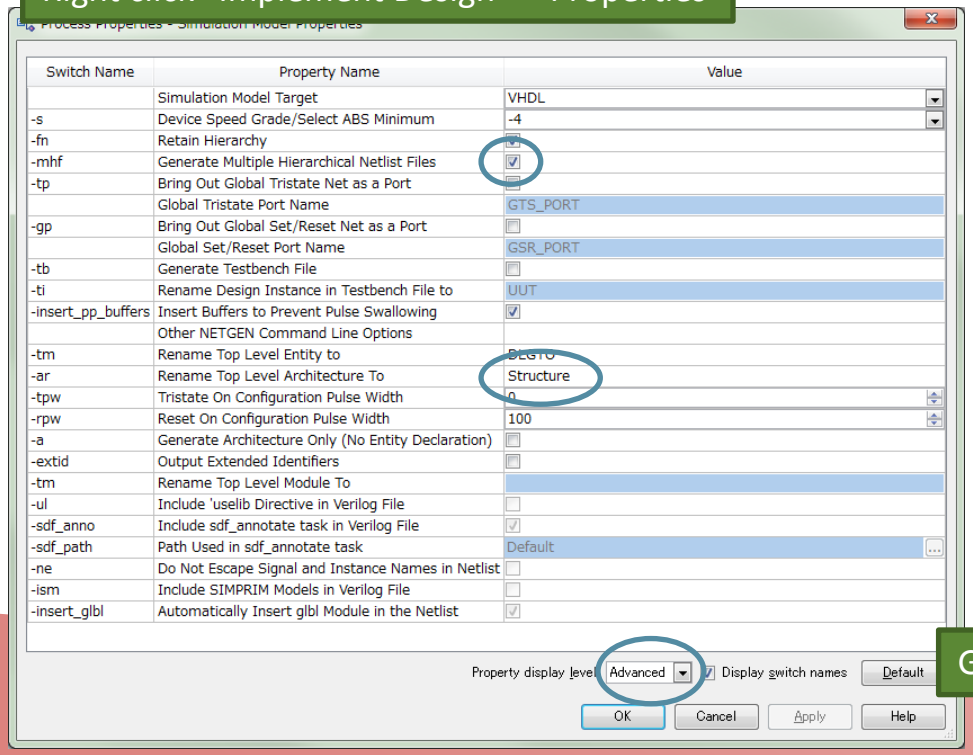
Important options

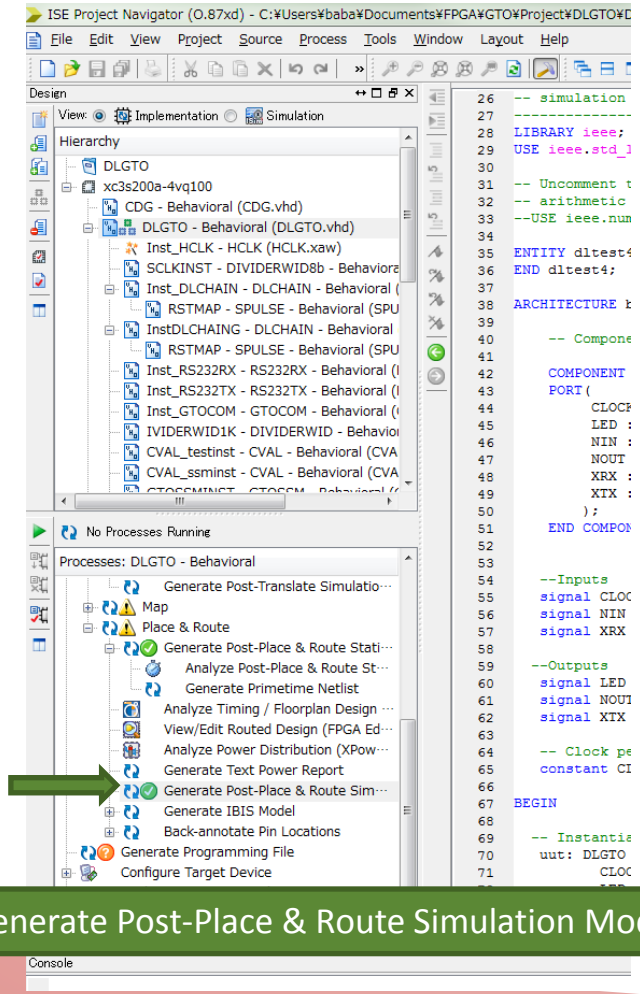


Simulation with Delay 1/3

We can simulate the delay of components and wires in FPGA

Right click “Implement Design” ->Properties

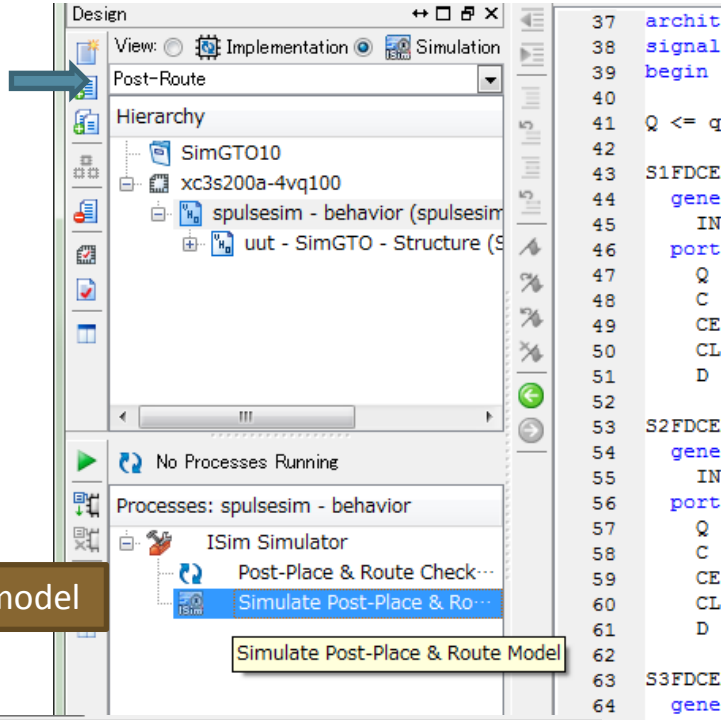




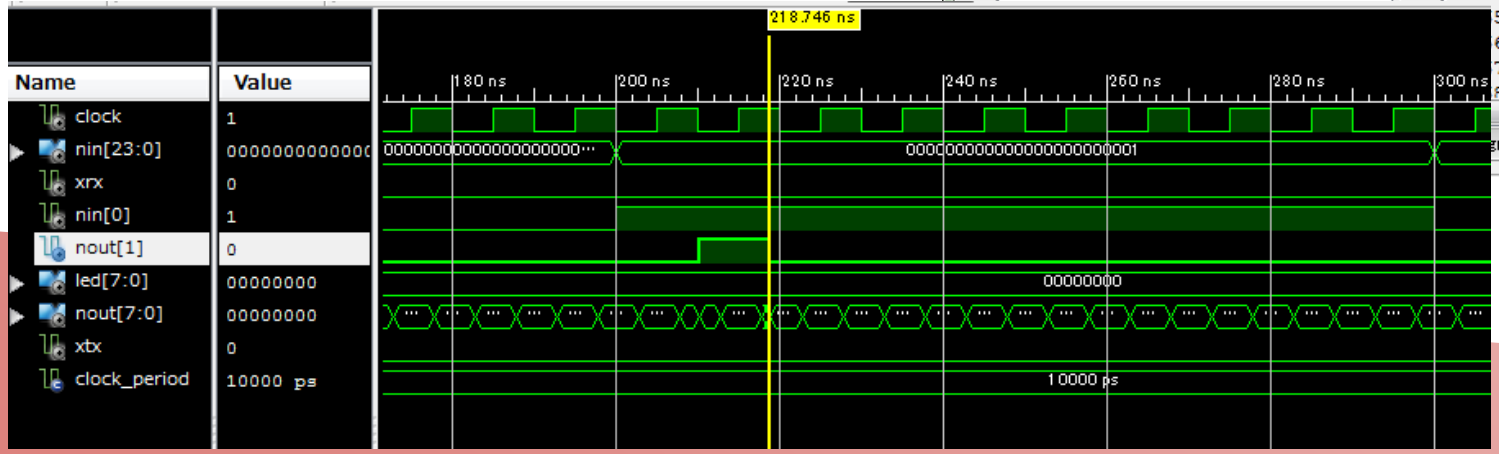
Generate Post-Place & Route Simulation Model

Simulation with Delay 2/3

Prepare usual test bench and choose “Post-Route” Simulation



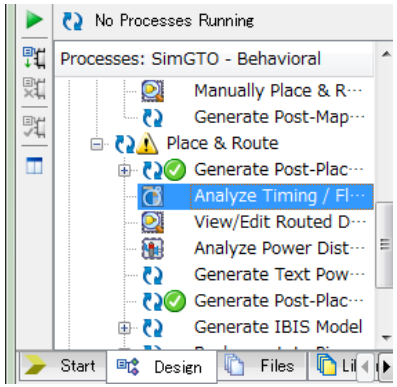
Do simulation as same as behavioral model



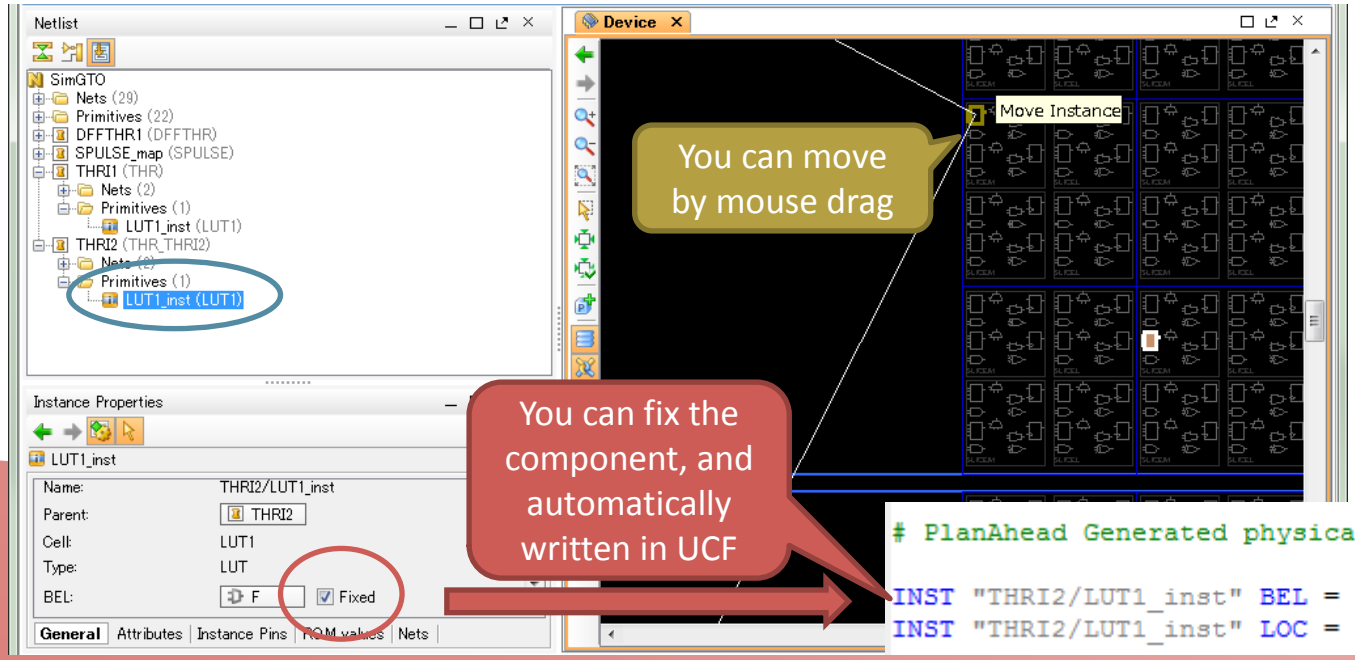
Simulation with Delay 3/3

Change the delay by moving components in FPGA. (example is LUT1)

```
library UNISIM;
use UNISIM.VComponents.all;

entity THR is
    Port ( s : in  STD_LOGIC;
           q : out  STD_LOGIC);
end THR;

architecture Behavioral of THR is

begin

  LUT1_inst : LUT1
  generic map (
    INIT => "10")
  port map (
    O => q,
    I0 => s
  );

end Behavioral;
```

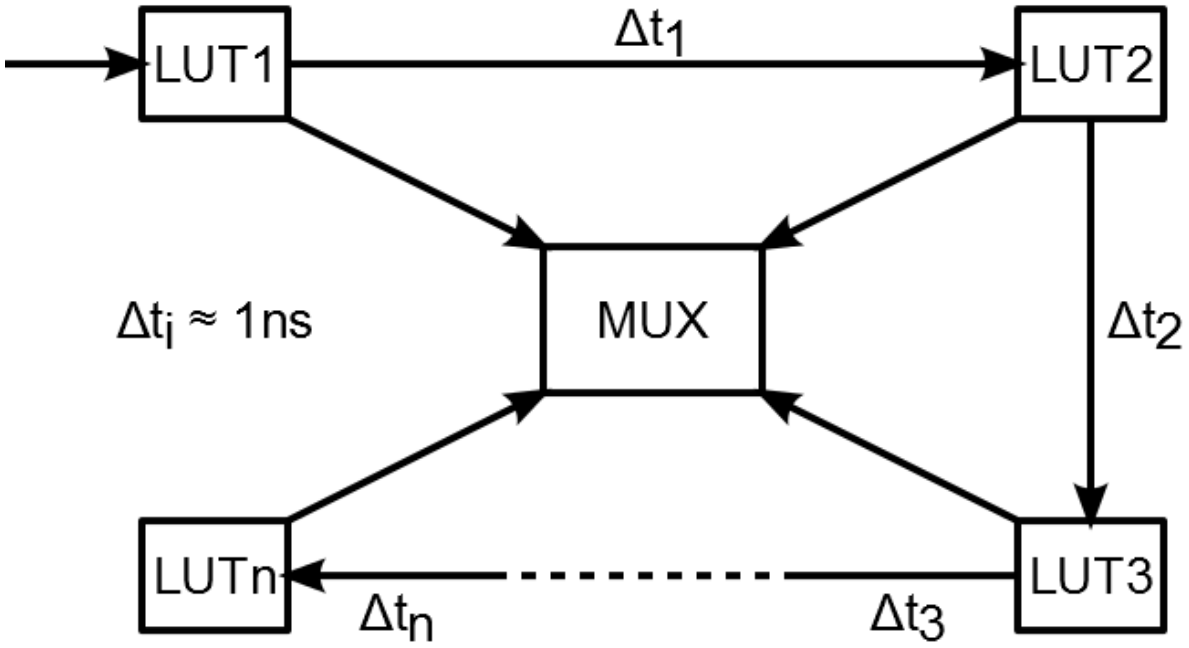


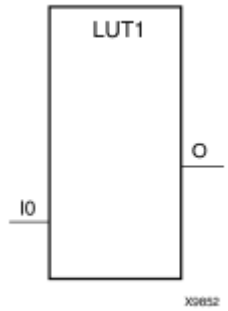
Launch PlanAhead




```
# PlanAhead Generated physical constraints

INST "THRI2/LUT1_inst" BEL = F;
INST "THRI2/LUT1_inst" LOC = SLICE_X30Y33;
```

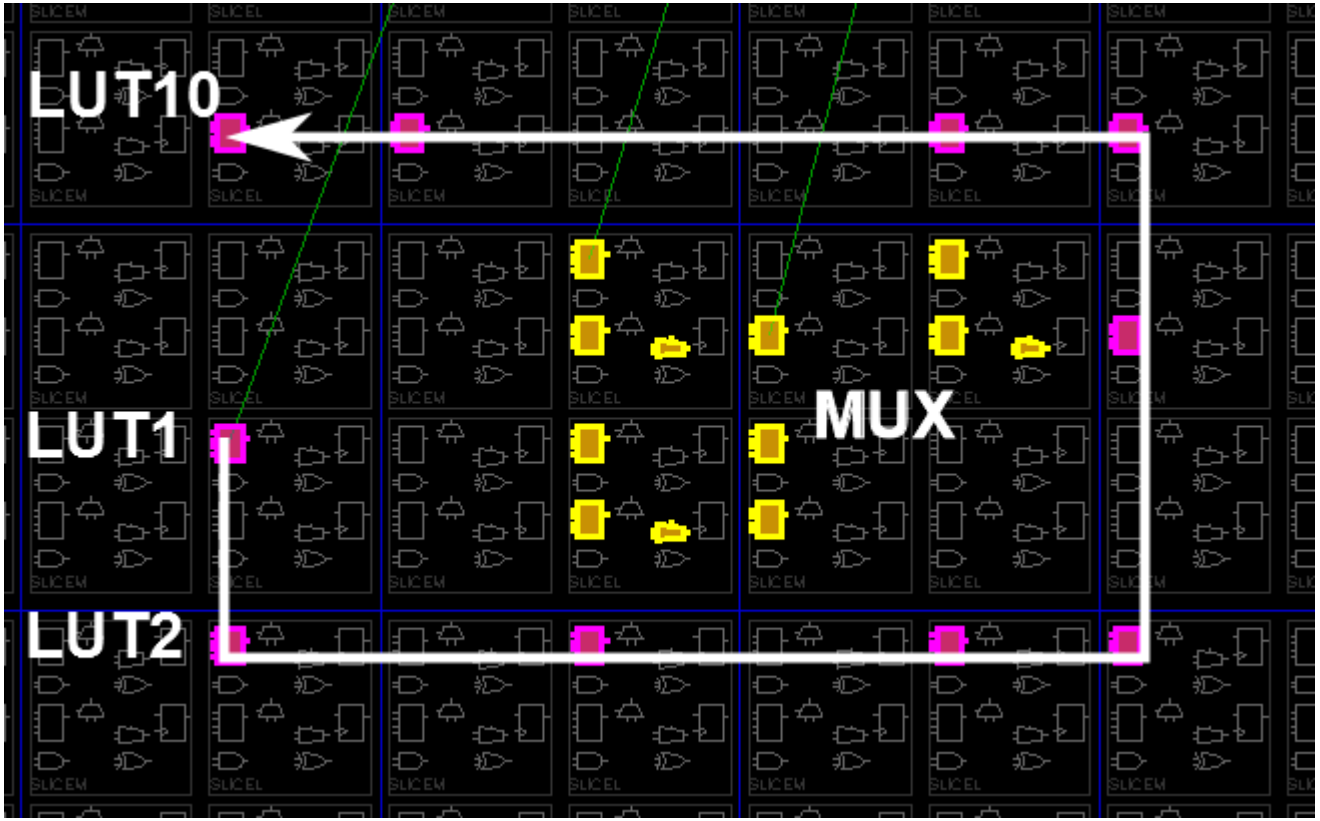
Logic delay by wiring 1/3





Logic delay by wiring 2/3

By floor planner



Logic delay by wiring 3/3

Example of UCF file

```
INST "Inst_delay2/LUT1_inst" BEL = G;
INST "Inst_delay2/LUT1_inst" LOC = SLICE_X7Y8;
INST "Inst_delay2/LUT2_inst" BEL = G;
INST "Inst_delay2/LUT2_inst" LOC = SLICE_X7Y7;
INST "Inst_delay2/LUT3_inst" BEL = G;
INST "Inst_delay2/LUT3_inst" LOC = SLICE_X9Y7;
INST "Inst_delay2/LUT4_inst" BEL = G;
INST "Inst_delay2/LUT4_inst" LOC = SLICE_X11Y7;
INST "Inst_delay2/LUT5_inst" BEL = G;
INST "Inst_delay2/LUT5_inst" LOC = SLICE_X12Y7;
INST "Inst_delay2/LUT6_inst" BEL = F;
INST "Inst_delay2/LUT6_inst" LOC = SLICE_X12Y9;
INST "Inst_delay2/LUT7_inst" BEL = F;
INST "Inst_delay2/LUT7_inst" LOC = SLICE_X12Y10;
INST "Inst_delay2/LUT8_inst" BEL = F;
INST "Inst_delay2/LUT8_inst" LOC = SLICE_X11Y10;
INST "Inst_delay2/LUT9_inst" BEL = F;
INST "Inst_delay2/LUT9_inst" LOC = SLICE_X8Y10;
INST "Inst_delay2/LUT10_inst" BEL = F;
INST "Inst_delay2/LUT10_inst" LOC = SLICE_X7Y10;
```

Some times, multiple LUTs packed into 1LUT.
To avoid this, hand-write constraints are required before floor planner.