

LUPO TimeStamp Module (Ver. 1.2)

Hidetada Baba

November 28, 2009

1 General

1.1 Function

This module is a CAMAC/VME LUPO module which including the functions of Time stamp, Output register and Interrupt register.

1.2 Time stamp

Time-stamp values are obtained with a 48 bits depth and a 10 ns resolution according to the trigger input (NIM IN1). It can be stored up to 1024 events into FIFO memory. Both clock sources of internal and external are available. In case of external clock, 100 MHz clock is generated by DLL (Delay Lock Loop) circuit from 25 MHz external clock of NIM ch3. The clear input (NIM IN2) reset the time-stamp value. By using this clear signal, the synchronization for all modules are achieved.

1.3 Output register

By the output register function, this module can output pulse and level signals from NIM OUT0–1. The pulse width is flexible, and it can be changed from 20 ns – 1.3 ms with 20 ns resolution.

1.4 Interrupt register

NIM IN0 input provides the interrupt signal to CAMAC and VME bus. The interrupt delay, which is a delay time between the signal timing and the interrupt generation timing, can be set from 20 ns to 1.3 ms with 20 ns step.

1.5 Indicator

1.5.1 Ex Clock OK

When the external clock is correct, this LED lights up. However even if the external clock is not 25 MHz, sometimes this LED becomes ON. And also, after the correct op-

eration, even if cable is removed, sometimes this LED still lights up. When the external clock mode, please check the Ex Clock through output by oscilloscope. If this signal is 25 MHz, the external clock synchronization is correct.

1.5.2 FIFO Full

There is FIFO memory, and it can store 1024 event time-stamp values. When FIFO becomes full, this LED will light up.

1.5.3 Int/Ext clock mode

With the external clock mode, this LED lights up. Internal clock mode case, this LED is off. The default setting is the external clock mode.

1.6 Connector

1.6.1 NIM input ch0 : Interrupt

CAMAC/VME interrupt signal is generated by this interrupt input. More than 20 ns width logic pulse is required.

1.6.2 NIM input ch1 : Trigger

Time stamp values are stored into FIFO according to this trigger input. More than 30 ns width logic pulse is required.

1.6.3 NIM input ch2 : Time Reset

With this input, time stamp values are cleared to be 0. This input is for the module synchronization. More than 20 ns width logic pulse is required.

1.6.4 NIM input ch3 : Ext Clock

Input external clock. Duty ratio 50:50, 25 MHz NIM logic pulse is needed.

1.6.5 NIM output ch0 : Output 0

An output for NIM level and pulse.

1.6.6 NIM output ch1 : Output 1

An output for NIM level and pulse.

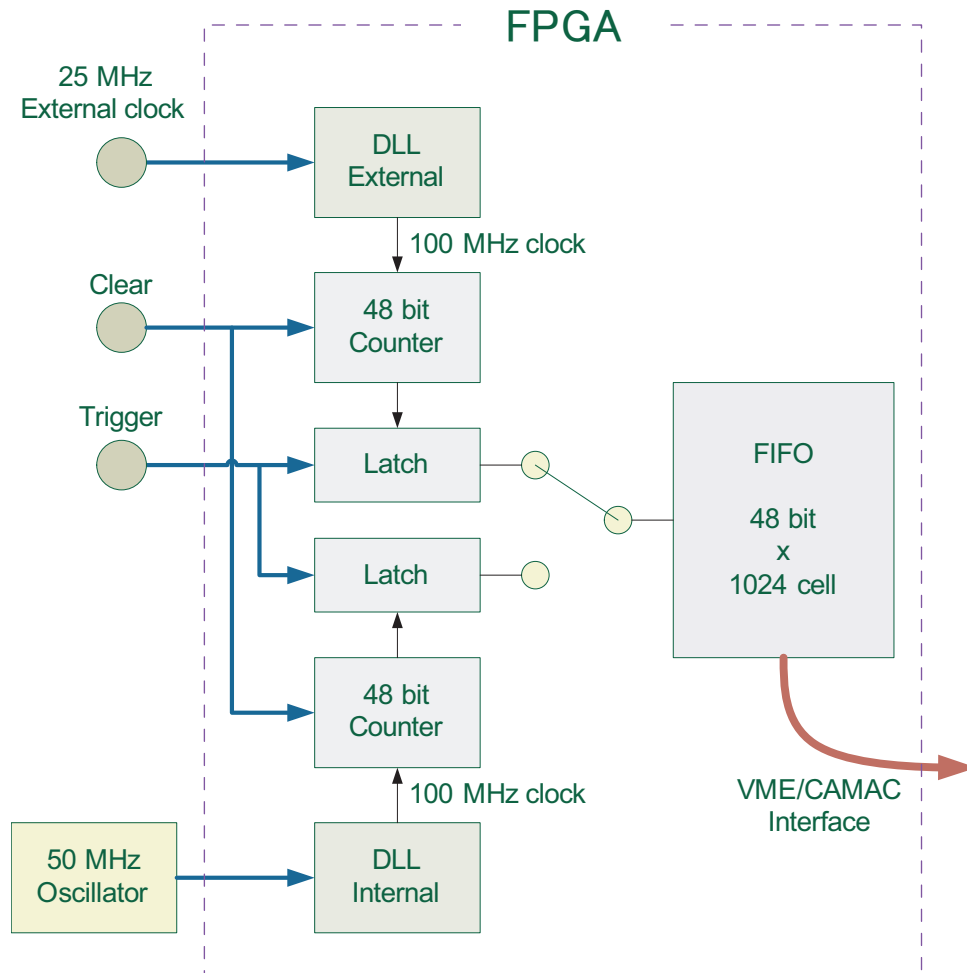
1.6.7 NIM output ch2 : Int clock through

An output of internal 25 MHz clock which is based on internal 50 MHz clock. This signal is used for synchronizing other modules.

1.6.8 NIM output ch3 : Ext clock through

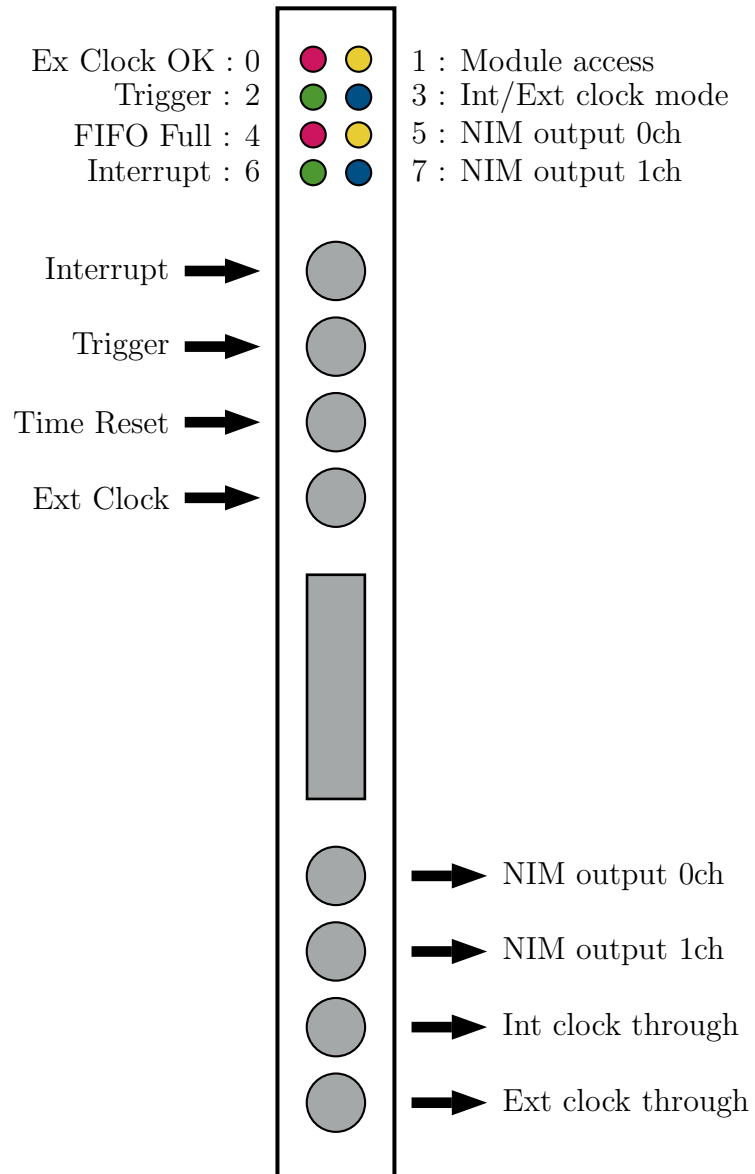
An output signal of external 25 MHz clock which is the through out of the external 25 MHz clock input. This signal is used for checking the external clock quality and synchronizing other modules. This through out is not a real direct output of the external clock. The external clock is put into the DLL circuit once, and this signal come from one of the DLL outputs. Thus, if the 25 MHz external clock has large noise, this through out will be not stable signal.

1.7 Block diagram



☒ 1.1: Block diagram of time stamping part.

1.8 Front panel



2 Interface

2.1 Register map

Command list.

CAMAC (R/W)	VME	Register	Data	VME R/W
F(0)A(0)	Base + %00	Data 24 bits lower	D32	read
F(0)A(2)	Base + %04	Data 24 bits higher	D32	read
F(0)A(4)	Base + %08	Data 32 bits lower	D32	read
F(0)A(6)	Base + %0c	Data 32 bits higher	D32	read
F(1)A(0)	Base + %10	Trigger Counter	D32	read
F(1)A(2)	Base + %14	FIFO Counter	D32	read
F(1)A(4)	Base + %18	Data on the fly	D32	read
F(2)A(0)	Base + %20	Data 24 bits sequential	D32	read
F(2)A(4)	Base + %24	Data 32 bits sequential	D32	read
F(16)A(0)	Base + %00	Level Output	D16	write
F(17)A(0)	Base + %10	Pulse Output	D16	write
F(4)A(0) F(20)A(0)	Base + %40	Pulse Width	D16	read/write
F(4)A(1) F(20)A(1)	Base + %42	Interrupt Delay	D16	read/write
F(6)A(0) F(22)A(0)	Base + %60	Clock Source	D16	read/write
F(7)A(0)	Base + %70	Module version	D16	read
F(9)A(0)	Base + %90	Clear FIFO & Interrupt	D16	read
F(9)A(1)	Base + %92	Reset Time Stamp	D16	read
F(9)A(2)	Base + %94	Clear Trigger Counter	D16	read
F(9)A(3)	Base + %96	Clear All	D16	read
F(10)A(0)	Base + %94	Clear Interrupt	D16	read
F(24)A(0)	Base + %80	Disable Interrupt	D16	write
F(26)A(0)	Base + %A0	Enable Interrupt	D16	write

2.1.1 Data lower 24 bits

Return the lower 24 bits time stamp value from FIFO.

2.1.2 Data lower 24 bits

Return the higher 24 bits time stamp value from FIFO. Reading of lower bits is required before reading higher bits.

2.1.3 Data lower 32 bits

Return the lower 32 bits time stamp value from FIFO. CAMAC case, this value will be cut 24 bits.

2.1.4 Data higher 32 bits

Return the higher 16 bits time stamp value from FIFO. Reading of lower bits is required before reading higher bits.

2.1.5 Data on the fly

Return the current time stamp counter (higher 24 bits).

2.1.6 Trigger Counter

Return the number of trigger input. The data depth is 32 bits for VME, 24 bits for CAMAC. By access of Clear Trigger Counter Register, this value will be cleared.

2.1.7 FIFO Counter

Return the number of time stamp data in FIFO. The data depth is 11 bits. And the maximum value is 1024.

2.1.8 Data 24 bits sequential

Under development.

2.1.9 Data 32 bits sequential

Under development.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														ch1	ch0

2.1.10 Level Output

Output level signals from NIM Output connectors (1=on, 0=off).

2.1.11 Pulse Output

Output pulse signals from NIM Output connectors (1=on, 0=off). With this pulse signal, level output will be canceled.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														ch1	ch0

2.1.12 Pulse Width

Set the width of the pulse output signal. 1 point corresponds to 20 ns. The default value is 10 = 200 ns. The maximum value is 65536 \simeq 1.3 ms.

2.1.13 Interrupt Delay

Set the delay time during interrupt input arrival time and actual interrupt generation. 1 point corresponds to 20 ns. The default value is 0 = 0 ns. The maximum value is 65536 \simeq 1.3 ms.

2.1.14 Clock Source

Choose the time stamp clock source. Default is the external clock.

0 : Internal Clock

1 : External NIM Input 0

2.1.15 Clear FIFO & Interrupt

Clear FIFO memory and interrupt signal. In case of VME, this function is invoked by read action.

2.1.16 Reset Time stamp

Reset the time stamp counter to 0. FIFO memory is also cleared. In case of VME, this function is invoked by read action.

2.1.17 Clear Trigger Counter

Clear the trigger counter only. In case of VME, this function is invoked by read action.

2.1.18 Clear All

Clear FIFO memory, interrupt signal, the trigger counter. The time stamp counter is not reset. In case of VME, this function is invoked by read action.

2.1.19 Clear Interrupt

Clear interrupt signal only. If CAMAC/VME interrupt signal is generated by this module, the clear interrupt function should be called from interrupt service routine. In case of VME, this function is invoked by read action.

2.1.20 Disable Interrupt

Disable VME/CAMAC interrupt. In case of VME, this function is invoked by write action. Any write value is acceptable.

2.1.21 Enable Interrupt

Enable VME/CAMAC interrupt. In case of VME, this function is invoked by write action. Any write value is acceptable.

2.1.22 Version

Return the version code of this module. The following is VME Time Stamp Ver 1.2 case.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAMAC/VME				Module ID				Ver X.X				Ver X.X			
2				2				1				2			

3 Appendix

3.1 Version Information

1.2 With FIFO version.

1.1 Without FIFO. To avoid noise problem, the external clock input channel is changed.

1.0 Initial version.

3.2 Comment

To synchronize with Techno-AP DSP Module, the frequency of the external clock is 25 MHz. This frequency can be able to change by FPGA program.