LUPO TimeStamp Module (Ver. 1.6)

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1 General

1.1 Function

This module is a CAMAC/VME LUPO module which including the functions of Time stamp, Output register and Interrupt register.

1.2 Time stamp

Time-stamp values are obtained with a 48 bits depth and a 10 ns resolution according to the trigger input (NIM IN1). It can be stored up to 1024 events into FIFO memory. In firmware version 1.6, the only external clock mode is available. To use internal clock, connect NIM output ch2 and NIM input ch3. In case of external clock, 100 MHz clock is generated by DLL (Delay Lock Loop) circuit from 25 MHz external clock of NIM input ch3. The clear input (NIM IN2) reset the time-stamp value. By using this clear signal, the synchronization for all modules are achieved.

1.3 Output register

By the output register function, this module can output pulse and level signals from NIM OUT0–1. The pulse width is flexible, and it can be changed from 20 ns – 1.3 ms with 20 ns resolution.

1.4 Interrupt register

NIM IN0 input provides the interrupt signal to CAMAC and VME bus. The interrupt delay, which is a delay time between the signal timing and the interrupt generation timing, can be set from 20 ns to 1.3 ms with 20 ns step. The interrupt is generated when the number of interrupt signals in the memory equals the value written in the Interrupt Counter Register.
1.5 Indicator

1.6 Connector

1.6.1 NIM input ch0 : Interrupt/Busy in

CAMAC/VME interrupt signal is generated by this interrupt input. More than 20 ns width logic pulse is required. When the use busy chain is ’1’, this input channel is used for an external busy input.

1.6.2 NIM input ch1 : Trigger

Time stamp values are stored into FIFO according to this trigger input. More than 30 ns width logic pulse is required. This minimum pulse width can be changed by setting the Trigger Width. If the Interrupt Source register is ’1’, this trigger input is also used as an interrupt input.

1.6.3 NIM input ch2 : Time Reset

With this input, time stamp values are cleared to 0. This input is for the module synchronization. More than 20 ns width logic pulse is required.

1.6.4 NIM input ch3 : External Clock

Input 25MHz external clock.

1.6.5 NIM output ch0 : Output 0

An output for NIM level and pulse.

1.6.6 NIM output ch1 : Output 1/Busy output

An output for NIM level and pulse. When the use busy chain is ’1’, this output channel is used for a busy output.

1.6.7 NIM output ch2 : Int clock through

An output of internal 25 MHz clock which is based on internal 50 MHz clock. This signal is used for synchronizing other modules.
1.6.8 NIM output ch3 : External clock output

Generate 25MHz clock from external clock input. This clock is used to check the external clock is accepted or not. Also, to synchronize other LUPO timestamp modules, this external clock output is used.

1.7 Block diagram

![Block diagram diagram](image)
1.8 Front panel

- Ex Clock OK: 0
- Trigger: 2
- Reset input: 4
- FIFO Full: 6

1: Module access
3: Int/Ext clock mode
5: Software Veto
7: Interrupt generate

- Interrupt/Busy in
- Trigger
- Time Reset
- External Clock

- NIM output 0ch
- NIM output 1ch/Buyt out
- Int clock through
- Trigger through
## 2 Interface

### 2.1 Register map

<table>
<thead>
<tr>
<th>CAMAC (R/W)</th>
<th>VME</th>
<th>Register</th>
<th>Data</th>
<th>VME R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>F(0)A(0)</td>
<td>Base + %00</td>
<td>Data 24 bits lower</td>
<td>D16 read</td>
<td></td>
</tr>
<tr>
<td>F(0)A(2)</td>
<td>Base + %04</td>
<td>Data 24 bits higher</td>
<td>D16 read</td>
<td></td>
</tr>
<tr>
<td>F(0)A(4)</td>
<td>Base + %08</td>
<td>Data 32 bits lower</td>
<td>D16 read</td>
<td></td>
</tr>
<tr>
<td>F(0)A(6)</td>
<td>Base + %0c</td>
<td>Data 32 bits higher</td>
<td>D16 read</td>
<td></td>
</tr>
<tr>
<td>F(1)A(0)</td>
<td>Base + %10</td>
<td>Trigger Counter</td>
<td>D32 read</td>
<td></td>
</tr>
<tr>
<td>F(1)A(2)</td>
<td>Base + %14</td>
<td>FIFO Counter</td>
<td>D32 read</td>
<td></td>
</tr>
<tr>
<td>F(1)A(4)</td>
<td>Base + %18</td>
<td>Data on the fly</td>
<td>D32 read</td>
<td></td>
</tr>
<tr>
<td>F(2)A(0)</td>
<td>Base + %20</td>
<td>Data sequential</td>
<td>D32 read</td>
<td></td>
</tr>
<tr>
<td>F(2)A(4)</td>
<td>Base + %28</td>
<td>Clock 10k</td>
<td>D32 read</td>
<td></td>
</tr>
<tr>
<td>F(16)A(0)</td>
<td>Base + %00</td>
<td>Level Output</td>
<td>D16 write</td>
<td></td>
</tr>
<tr>
<td>F(17)A(0)</td>
<td>Base + %10</td>
<td>Pulse Output</td>
<td>D16 write</td>
<td></td>
</tr>
<tr>
<td>F(4)A(0)</td>
<td>F(20)A(0)</td>
<td>Base + %40</td>
<td>Pulse Width</td>
<td>D16 read/write</td>
</tr>
<tr>
<td>F(4)A(1)</td>
<td>F(20)A(1)</td>
<td>Base + %42</td>
<td>Interrupt Delay</td>
<td>D16 read/write</td>
</tr>
<tr>
<td>F(4)A(2)</td>
<td>F(20)A(2)</td>
<td>Base + %44</td>
<td>Interrupt Counter</td>
<td>D16 read/write</td>
</tr>
<tr>
<td>F(4)A(4)</td>
<td>F(20)A(4)</td>
<td>Base + %48</td>
<td>Interrupt Source</td>
<td>D16 read/write</td>
</tr>
<tr>
<td>F(4)A(5)</td>
<td>F(20)A(5)</td>
<td>Base + %4a</td>
<td>Use busy chain</td>
<td>D16 read/write</td>
</tr>
<tr>
<td>F(7)A(0)</td>
<td>Base + %70</td>
<td>Module version</td>
<td>D16 read</td>
<td></td>
</tr>
<tr>
<td>F(9)A(0)</td>
<td>Base + %90</td>
<td>Clear FIFO &amp; Interrupt</td>
<td>D16 read</td>
<td></td>
</tr>
<tr>
<td>F(9)A(1)</td>
<td>Base + %92</td>
<td>Reset Time Stamp</td>
<td>D16 read</td>
<td></td>
</tr>
<tr>
<td>F(9)A(2)</td>
<td>Base + %94</td>
<td>Clear Trigger Counter</td>
<td>D16 read</td>
<td></td>
</tr>
<tr>
<td>F(9)A(3)</td>
<td>Base + %96</td>
<td>Clear All</td>
<td>D16 read</td>
<td></td>
</tr>
<tr>
<td>F(9)A(4)</td>
<td>Base + %98</td>
<td>Clear Interrupt</td>
<td>D16 read</td>
<td></td>
</tr>
<tr>
<td>F(24)A(0)</td>
<td>Base + %80</td>
<td>Disable Interrupt</td>
<td>D16 write</td>
<td></td>
</tr>
<tr>
<td>F(26)A(0)</td>
<td>Base + %A0</td>
<td>Enable Interrupt</td>
<td>D16 write</td>
<td></td>
</tr>
</tbody>
</table>
2.1.1 Data on the fly

Return the current time stamp counter (higher 24 bits).

2.1.2 Trigger Counter

Return the number of trigger input. The data depth is 32 bits for VME, 24 bits for CAMAC. By access of Clear Trigger Counter Register, this value will be cleared.

2.1.3 Level Output

Output level signals from NIM Output connectors (1=on, 0=off).

2.1.4 Pulse Output

Output pulse signals from NIM Output connectors (1=on, 0=off). With this pulse signal, level output will be canceled.

2.1.5 Pulse Width

Set the width of the pulse output signal. 1 point corresponds to 20 ns. The default value is 10 = 200 ns. The maximum value is $65536 \approx 1.3$ ms.

2.1.6 Interrupt Delay

Set the delay time during interrupt input arrival time and actual interrupt generation. 1 point corresponds to 20 ns. The default value is 0 = 0 ns. The maximum value is $65536 \approx 1.3$ ms.
2.1.7 Interrupt Counter

When the interrupt input (or trigger input when Interrupt source register is ‘1’) reaches this number, IRQ signal is generated. This register accepts up to 0–2047 (0 corresponds to 2048). If the value of the busy chain register is ‘1’, busy signal is generated until interrupt is cleared.

2.1.8 Interrupt Source

In the default setting, interrupt source is NIM input 0. When write ‘1’ on this register, the interrupt source is switched to the trigger input.

2.1.9 Use busy chain

When 0th bit has the value = ‘1’, the busy chain mode is enabled. NIM input 0 is used as external busy input. NIM output 1 is busy signal. The busy signal consists of OR of external busy input, IRQ signal and 1th bit of this register. Once, interrupt occurs, the busy signal is latched until clear interrupt. When 1th bit is ‘1’, the busy signal is forced to be high.

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
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<td></td>
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<tr>
<td>1</td>
<td>0</td>
<td>force</td>
<td>use</td>
<td></td>
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</table>

2.1.10 Clear FIFO & Interrupt

Clear FIFO memory and interrupt signal. In case of VME, this function is invoked by read action.

2.1.11 Reset Time stamp

Reset the time stamp counter to 0. FIFO memory is also cleared. In case of VME, this function is invoked by read action.

2.1.12 Clear Trigger Counter

Clear the trigger counter only. In case of VME, this function is invoked by read action.
2.1.13 Clear All

Clear FIFO memory, interrupt signal, the trigger counter. The time stamp counter is not reset. In case of VME, this function is invoked by read action.

2.1.14 Clear Interrupt

Clear interrupt signal only. If CAMAC/VME interrupt signal is generated by this module, the clear interrupt function should be called from interrupt service routine. In case of VME, this function is invoked by read action.

2.1.15 Disable Interrupt

Disable VME/CAMAC interrupt. In case of VME, this function is invoked by write action. Any write value is acceptable.

2.1.16 Enable Interrupt

Enable VME/CAMAC interrupt. In case of VME, this function is invoked by write action. Any write value is acceptable.

2.1.17 Version

Return the version code of this module. The following is VME Time Stamp Ver 1.6 case.

<table>
<thead>
<tr>
<th>15</th>
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<th>13</th>
<th>12</th>
<th>11</th>
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<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAMAC/VME</td>
<td>Module ID</td>
<td>Ver X.X</td>
<td>Ver X.X</td>
<td></td>
<td></td>
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</tbody>
</table>
3 Appendix

3.1 Version Information

1.6 With FIFO, Interrupt count, Busy output, No Internal clock mode

1.5 50MHz LVDS external clock, Without FIFO

1.2 With FIFO

1.1 Without FIFO, stable version